THE ELECTRONICS MAGAZINE WITH THE PRACTICAL APPROACH

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Elektor Electronics

ATN-Filmnet decoder
Centronics buffer
VHF/UHF wide-band amplifiers
Power line modem
Video recording amplifier
Dealing with e.m.i.
Practical filter design
Battery 'low' indicator

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Elektor Electronics

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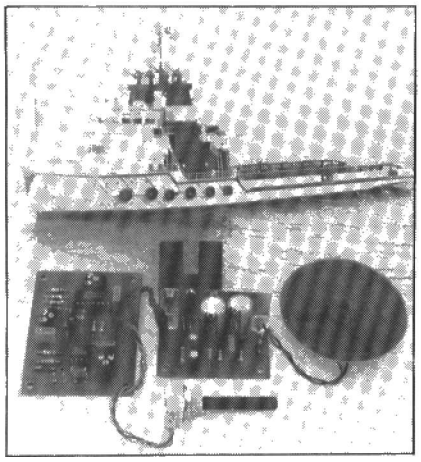

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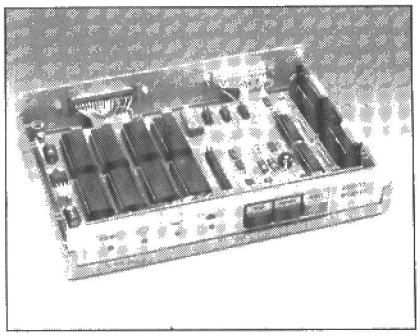

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- Protection devices for loudspeaker systems
- Multi-point infra-red control
- Video recording amplifier*
- Satellite sub-woofer system
- Rock-steady 10 MHz signal from DLF
- RDS decoder

* We regret that owing to unforeseen circumstances this article could not be included in this issue.

Front cover

The ghostly figure, known as the Head and Torso Simulator (HATS), seen here being fitted with a telephone handset by technician Helen Christian, is used in tests at British Telecom's Research laboratories to measure sound pressure.
The tests take place in an anechoic chamber. An artificial ear on the simulator holds a miniature microphone to monitor the loudness and frequency response of the telephone.

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ELECTRONICS IN THE NORTH OF ENGLAND

The North of England offers an exceptional environment for the electronics industry. At present over 200 companies operate in the region, spread across all sectors of the industry. Home grown talent includes established names like NEI Electronics, Elmwood Sensors and Seaward Electronics. Multinationals from other countries, including Sanyo, Samsung, Goldstar and Electrolux have chosen the North of England as a base for their United Kingdom or European operations because they recognize the advantages of a well-trained and flexible workforce, and the good communications the region can offer them. Underpinning the industry in the region is a wealth of first-rate component suppliers and academic expertise, both in terms of research and graduate output, that rival those of any other part of the country.

The region is ideal for nurturing the smaller, expanding company, as well as supporting the large manufacturing organizations that have either grown up in it or selected it as a base for their operations. For instance, Canford Audio, which started life in Washington, Tyne & Wear, is establishing a first-class reputation in the professional audio field, while Stadium Electronics expanded from its base in Enfield into a purpose-built factory in Hartlepool.

The region's expertise in processing and displaying information is demonstrated by the many successful large-scale display systems installed on road sides and sports grounds throughout the world by NEI Displays and Wearside Electronics, a division of the Edward Thomson Group. Both Durham University and Sunderland Polytechnic are engaged in research into digital systems. At Durham, research is being carried out on adaptive optics for rapid image processing and control.

The academic institutions in the North of England: universities at Durham and Newcastle, and polytechnics at Newcastle, Sunderland and Teesside work closely with industry on a regional, national and international level. In addition to producing a well-equipped workforce for the electronics industry, they offer their expertise in research and problem solving to industry. Durham University alone has external contracts for R&D in excess of £5 million, much of which is work on ASIC design and electronics materials. Newcastle University has acknowledged strengths in VLSI design and digital control techniques. Sunderland Polytechnic offers special services through the Magnet Centre and in design software. Newcastle Polytechnic carries out research into communications and microprocessor systems. Teesside Polytechnic is renowed for its work on CAD techniques.

One reason that electronic companies have prospered in the region is the excellent support available from local providers of production services and supplies. Newcastle University and the North East Regional Electronics Centre both offer integrated circuit design services. A whole host of companies supply specialist PCB design services. Peak Production Services, yet another new arrival to the region, provide specialist test fixing services, while complete assemblies can be built using power supplies from Keland Electronics and cord sets from Feller (UK) Ltd.

Source: Northern Development Company • Bank House • Carliol Square • Newcastle-upon-Tyne NE1 6XE.

ELECTRONICS SCENE

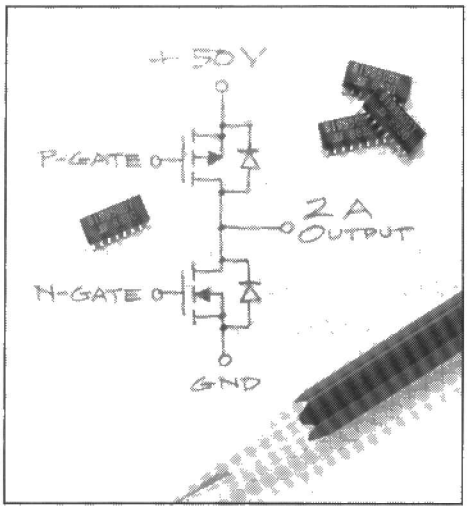
SIMPLER TRACKER BALL FOR ATARI ST

Hero Electronics have advised that the "Tracker Ball for Atari ST" may be simplified by replacing the CNY37 and 40106 by a Sharp "Opic" photo-interrupter. That device contains emitter, sensor, Schmitt trigger, output transistor and voltage regulator, all in one package, available from **Hero Electronics Ltd • Dunstable Street • Ampthill • Bedfordshire MK45 2JS • Telephone (0525) 405015.**

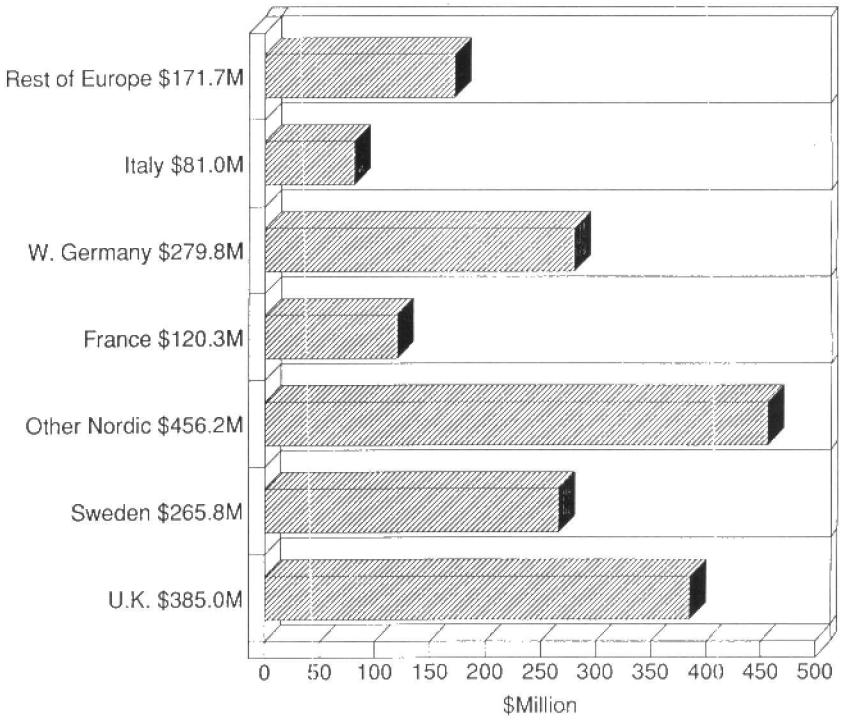
SPACE LASER COMMUNICATIONS

Marconi Space Systems is to investigate the feasibility of using advanced laser systems as an alternative to microwave links for inter-satellite communications. Space communication links will be essential in the future to maintain continuous contact with low-earth-orbiting spacecraft such as the space station elements or earth observation satellites to enable the transfer to the ground of the large quantities (100 Mb/s and more) of data they generate. Laser communications offer significant advantages over conventional microwave links in the size and mass of hardware, as well as in their virtually unlimited bandwidth and carrying capacity.

The Si9950DY half-bridge driver from Siliconix, which includes a complementary pair of *n*-channel and *p*-channel MOSPOWER transistors, is assembled in a 16-pin small-outline package with a copper leadframe designed to provide optimum thermal performance of board-mounted applications. This compact device saves valuable board space by replacing two MOSFET packages with one, and allows the use of automated surface-mount assembly techniques. (*Photo courtesy of Siliconix*).



CELLULAR COMMUNICATIONS MARKET IN EUROPE - 1988



According to a report from Frost & Sullivan, *The Cellular Communications Market in Europe*, explosive demand for mobile telecommunications services in Europe will drive the market for cellular terminals past the $3 billion per year mark by 1993, despite inadequate system planning in West Germany and France, which is expected to hold capacity in the cities of those countries well below consumer demand into the 1990s.

WAY CLEAR FOR WALL PICTURE TELEVISION

A television set that can be hung on the wall like a picture is now possible following the development by Rytrack of Liverpool of a new method of producing flat screens.

The development, which allows the manufacture of liquid crystal display (LCD) screens as thin as a sheet of glass, has wide-ranging implications, not only for television sets, but also for cockpit and dashboard displays, art reproduction and instant colour photocopiers.

The development is based on the use of polysilicon instead of amorphous silicon for the transistors. Rytrack has developed a fully automated chemical-vapour-deposition (CVD) machine that can produce flat screens up to 355×355 mm on a commercial basis. Existing technology has so far come up with pocket-sized versions only.

FACSIMILE OVER RADIO LINKS

Facsimile transmissions can be made over radio links with standard Group III machines with the aid of a buffer unit developed by Intertec of Wimborne. Type-coded B426, the buffer unit is designed for use with standard machines fitted with simplex radio-bearer circuits, while the serial data output format is also suitable for direct connection to a digital network.

In operation, the unit interfaces, via an integral V29/V27 modem, to any industry-standard Group III desktop fax machine. Connection to the radio equipment is by a separate suitable modem that should incorporate FEC or SELFEC functions for optimum error correction. A combined "radiofax" modem (Model RF726) is also available.

YOUNG ELECTRONIC DESIGNER AWARDS 1989

The 1989 Young Electronic Designer Awards (YEDA) schema has won the enthusiastic backing of the Confederation of British Industry (CBI) and renewed sponsorship from semiconductor and computer manufacturers Texas Instruments Ltd, and electronics distributors Cirkit Holdings PLC.

The scheme is open to students at secondary schools, polytechnics and universities throughout the United Kingdom who compete in three categories: Junior (under 15); Intermediate (15—17 years incl.); and Senior (18—25 years incl.).

ELECTRONICS SCENE

TOTAL EUROPEAN SEMICONDUCTOR MARKET
(MILLIONS OF US DOLLARS)

1987 RANK	1988 RANK	RANKED COMPANIES	1987	1988	ANNUAL GROWTH (%)
1	1	PHILIPS	930	1,002	7.7
2	2	SGS THOMSON	537	650	21.0
3	3	TEXAS INSTRUMENTS	492	636	29.3
4	4	MOTOROLA	478	616	28.9
5	5	SIEMENS	475	571	20.2
7	6	INTEL	283	485	71.4
6	7	NATIONAL SEMICONDUCTOR	345	390	13.0
8	8	NEC	249	370	48.6
12	9	TOSHIBA	188	349	85.6
10	10	AMD	235	279	18.7
13	11	HITACHI	157	246	56.7
9	12	ITT	243	246	1.2
11	13	TELEFUNKEN	209	230	10.0
14	14	PLESSEY	151	198	31.1
15	15	GE SOLID STATE	122	141	15.6
29	16	SAMSUNG	35	134	282.9
16	17	FUJITSU	110	131	19.1
17	18	ASEA BROWN BOVERI	91	100	9.9
18	19	ANALOG	77	96	24.7
20	20	MITSUBISHI	53	86	62.3

SEMICONDUCTOR WORLD MARKET

Dataquest's preliminary 1988 worldwide semiconductor market share survey shows that the worldwide market growth in the semiconductor industry slowed in the fourth quarter of 1988 after a very strong showing in the first three quarters of the year, resulting in a total market growth of 32.9 per cent (compared with 22.8 per cent growth in 1987).

However, 1988 was a high-growth year for the European semiconductor market. Dataquest estimates that the European semiconductor market grew by 33.6 per cent (up to $8,491 million in 1988 from $6,355 million in 1987).

The basic challenge of the scheme is for students to produce an electronic device of their own which is original, effective and has a useful application in everyday life. A prestigious trophy and valuable cash prizes are presented to the winners in each category. Furthermore, for competitors in the senior age group there are the prospects of a job in electronics and course sponsorship.

VIDEO TIMECODE READER

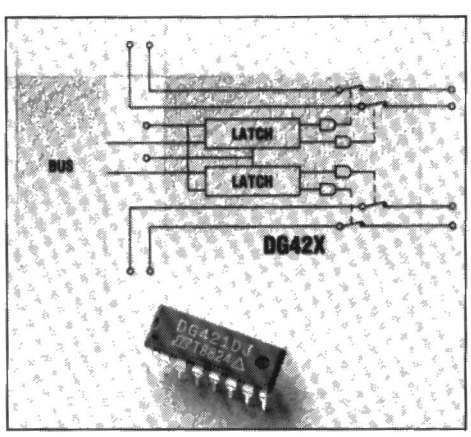
Two video timecode reader/inserter units for video distribution systems, models TRE3204L and TRE3204V, are available from Avitel Electronics of Beckenham. The plug-in units are intended for inclusion in video distribution systems associated with edit suites, or for similar applications where compactness and the facility for rapid selection of input sources are desirable. They are controlled from the front panel, although remote control facilities are also available. It is possible to display timecode only, user bits only, or both together.

UK MEDICAL IMAGING KNOW-HOW FOR TOSHIBA

Toshiba, Japan's third largest electrical and electronics company, is to build magnetic resonance imaging (MRI) machines based on British technology.

Under a licensing deal recently concluded with the British Technology Group (BTG), Toshiba has acquired the right to manufacture and distribute machines that use BTG's MRI know-how that is covered by patents in Japan and the rest of the world.

Magnetic resonance imaging is described as one of the major advances in medical diagnosis this century, comparable in importance with the discovery of X-rays. It is now used routinely to generate detailed pictures of tissues deep in the human body. MRI relies on exciting the nucleii and reading the emitted signals in the presence of gradient magnetic fields. The resonance signals are then analysed to give a detailed picture of the anatomy of the region under examination.



The high-performance silicon-gate DG400 family from Siliconix includes three dual analogue switches with on-board data latches. The DG421, DG423 and DG425 simplify bus interface designs by eliminating the need of external latches, thus saving both board space and components costs. (*Photo courtesy of Siliconix*).

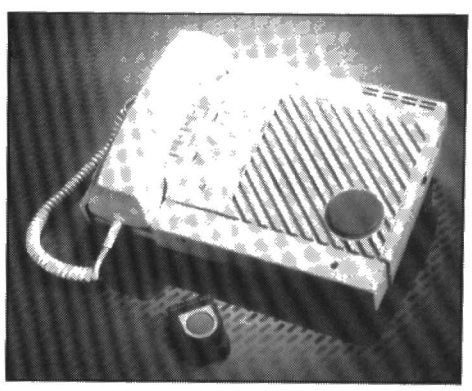
COMMUNICATION AID FOR THE SPEECH IMPAIRED

Instant communication for those who can not speak is made easier with the aid of a unit designed by Toby Churchill of Cambridge. The "Lightwriter SL1" is a lightweight, rugged, battery-powered unit that instantly displays what is entered on its typewriter-style keyboard. The message is shown simultaneously on two liquid crystal displays: one facing the user and the other facing away for anyone to read.

TWO-WAY SPEECH EMERGENCY ALARM

A community alarm system for the elderly and disabled, developed by Tunstall of Whiteley Bridge, Yorkshire, includes a small body-worn trigger device that allows two-way speech communication even if the user is some distance from the unit.

The "Piper Lifeline II" combines a mains-operated emergency communication unit with a modern push-button telephone. The trigger device sends a radio signal to the unit when a button is pressed, which automatically contacts a control centre or warden and identifies the caller. Two-way speech between control centre and user is possible, and the device may also be used as a cordless method of answering the telephone.



POWER LINE MODEM

The NE5050 from Philips Components has been designed for sending and receiving data over the AC mains network, coaxial cables or twisted-pair cables. The modem described here is a mains-based application of the NE5050. It works in conjunction with an error-correcting computer program for exchanging data or remote control of equipment.

by J. Bareford

A modem (acronym for MOdulator/DEModulator) is almost invariably used where the distance between computers, or a computer and peripheral equipment, exceeds the capabilities of the well-known RS-232 interface with associated cables. In practice, this means that some sort of modem is necessary when the data rate and distance exceed 1200 baud and about 30 metres respectively. In most cases, the modem is located physically close to the computer or peripheral (sometimes it is internal to it). Modems generally use frequency-shift-keying (FSK) of a carrier to convert the logic levels received from the computer's RS-232 outlet into tones that can be carried over, say, the telephone network. In receive mode, the tones from the modem at the other end of the line are demodulated and converted to RS-232 levels for sending to the computer.

The present modem does not use FSK, but ASK (amplitude shift keying) for reasons discussed below. Similar to certain types of intercom, the NE5050-based modem is connected to the remote station via the mains network.

Background to amplitude shift keying

The mains network is by no means ideal for data communication. Impulse noise, voltage dips, line impedance modulation and high-frequency signals are but a few of the sources of interference to be taken into account. Improperly decoupled fluorescent tubes, dimmers, refrigerators and washing machines are notorious for the high levels of 'mains pollution' they cause.

Clearly, the design of a practical mains modem should anticipate high levels of interference and possible corruption of data owing to the above appliances.

In radio technology, it has been known for almost 100 years that CW (*continuous wave* or modulation type A1), or simply switching the transmitter on and off, is the simplest, yet most interference-resistent, modulation method available. Figure 1 shows how CW is used by the present modem — a 120 kHz carrier is generated and digital input data determines when the carrier is to be superimposed on to the mains lines. Collision, or more precisely *summing* of data, however, occurs when two modems connected to the network

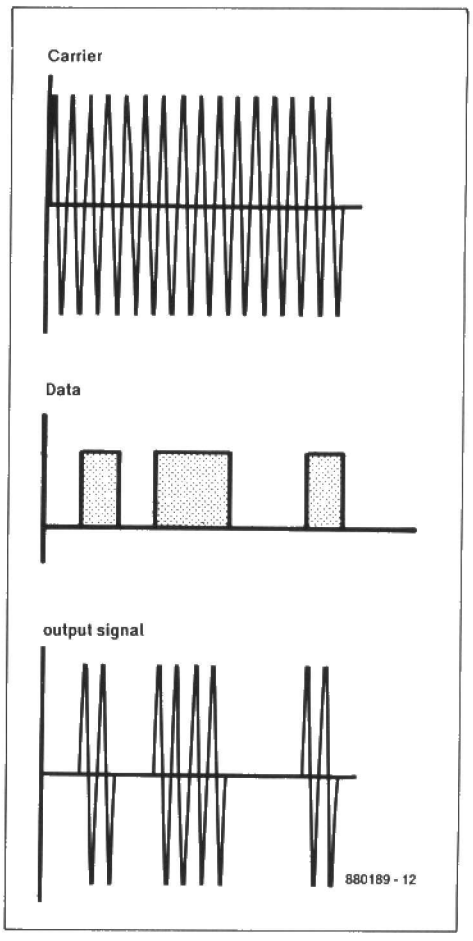


Fig. 1. The modem uses amplitude-shift keying (ASK) for sending data via the mains network.

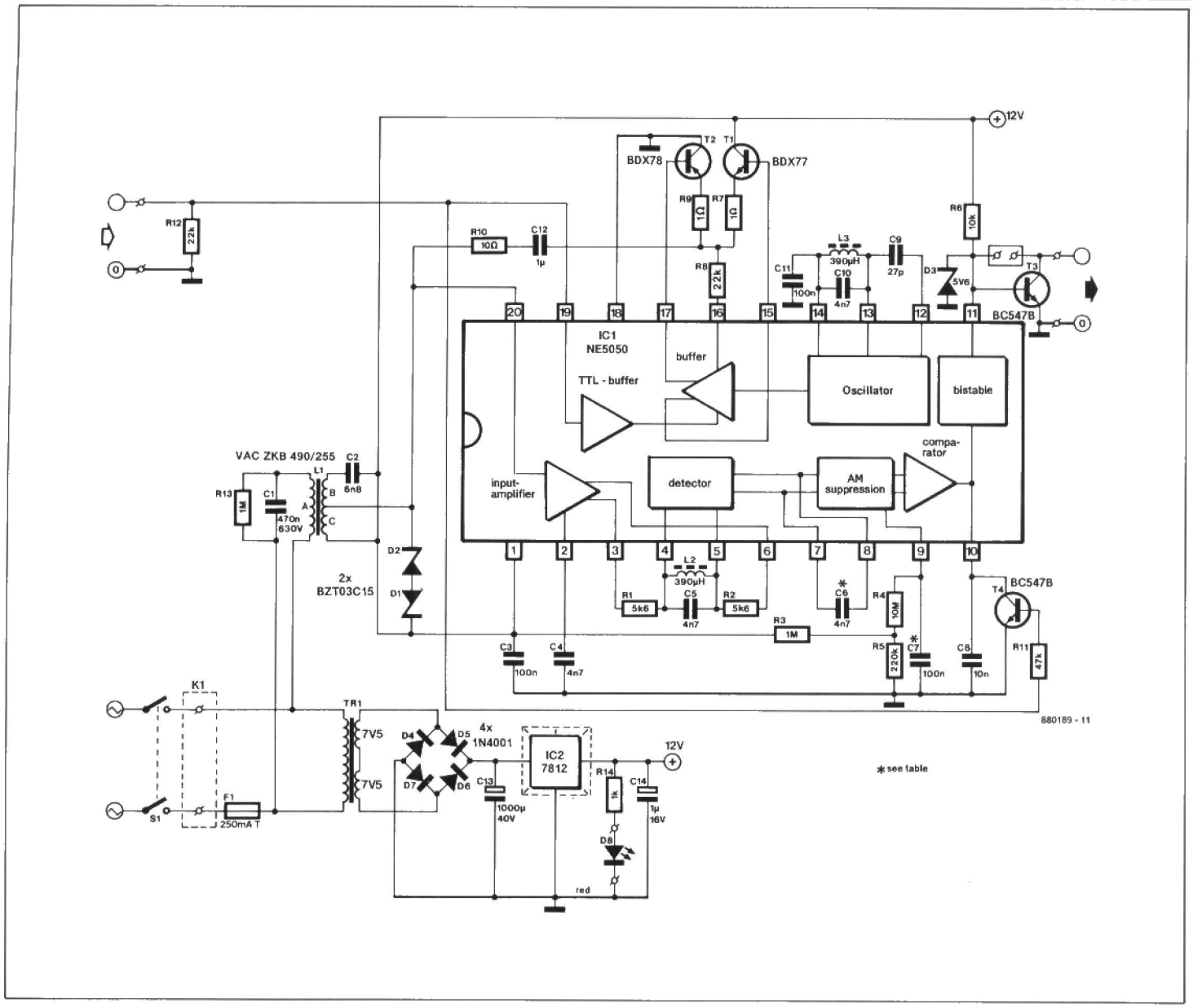


Fig. 2. Circuit diagram of the power-line modem.

transmit simultaneously. Thanks to the use of ASK, this only leads to distortion of data, not to overloading of the modem input. By setting up an error-detecting data exchange protocol in the computer, messages between modems can be repeated until they are correctly received. The use of a communications program on the computer for combatting data collision and interference simplifies the modem hardware considerably, and at the same time makes it virtually computer-independent.

An integrated modem

Apart from the electrical connection and the component values, the circuit diagram of Fig. 2 shows the internal structure of the central part, the NE5050 in position IC_1.

The transmitter in the modem chip is composed of a carrier oscillator, a TTL buffer/input amplifier, and a line driver that also functions as the amplitude-modulator. External components C_9, C_{10} and L_3 tune the oscillator to 120 kHz. Capacitor C_{11} does not form part of the tuned circuit, but serves to decouple the internally generated supply voltage of $\frac{1}{2}U_b$ which is used for biasing the oscillator. The generated carrier is applied to the line driver in which amplitude modulation takes place. The carrier is modulated by the data signal applied to pin 19 of the chip. Together with T_1, T_2, R_7, R_8 and R_9, the driver forms a class-AB output stage that gives the ASK signal enough power to be superimposed on to the mains lines. For reasons of safety, this is done with the aid of a double-insulated line transformer with a turns ratio L_{1a}:L_{1b}:L_{1c}=1:4:1. A number of components with specific functions are arranged around this transformer. C_{12} and R_{10} ensure a sufficiently high termination impedance for the line driver. C_1 suppresses the mains frequency (50 or 60 Hz), and D_1 and D_2 have the double function of transient suppressor and limiter for the received 120 kHz signal. Under no conditions should the indicated diodes be replaced by common zener diodes which these are far too slow in this application, and, therefore, unable to protect the mains modem chip from damage by voltage surges.

The input of the modem, pin 20, normally receives not only the signals from

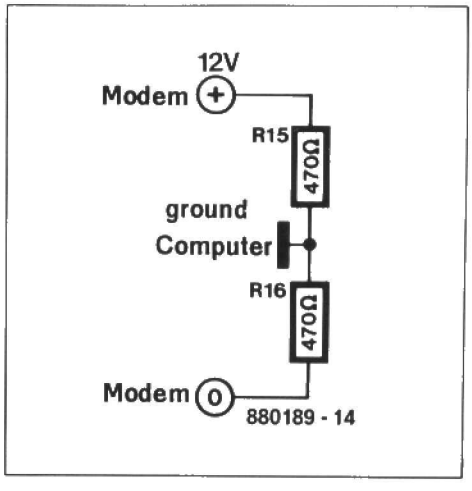


Fig. 3. Simple extension of the modem interface to enable connection to an RS-232 outlet.

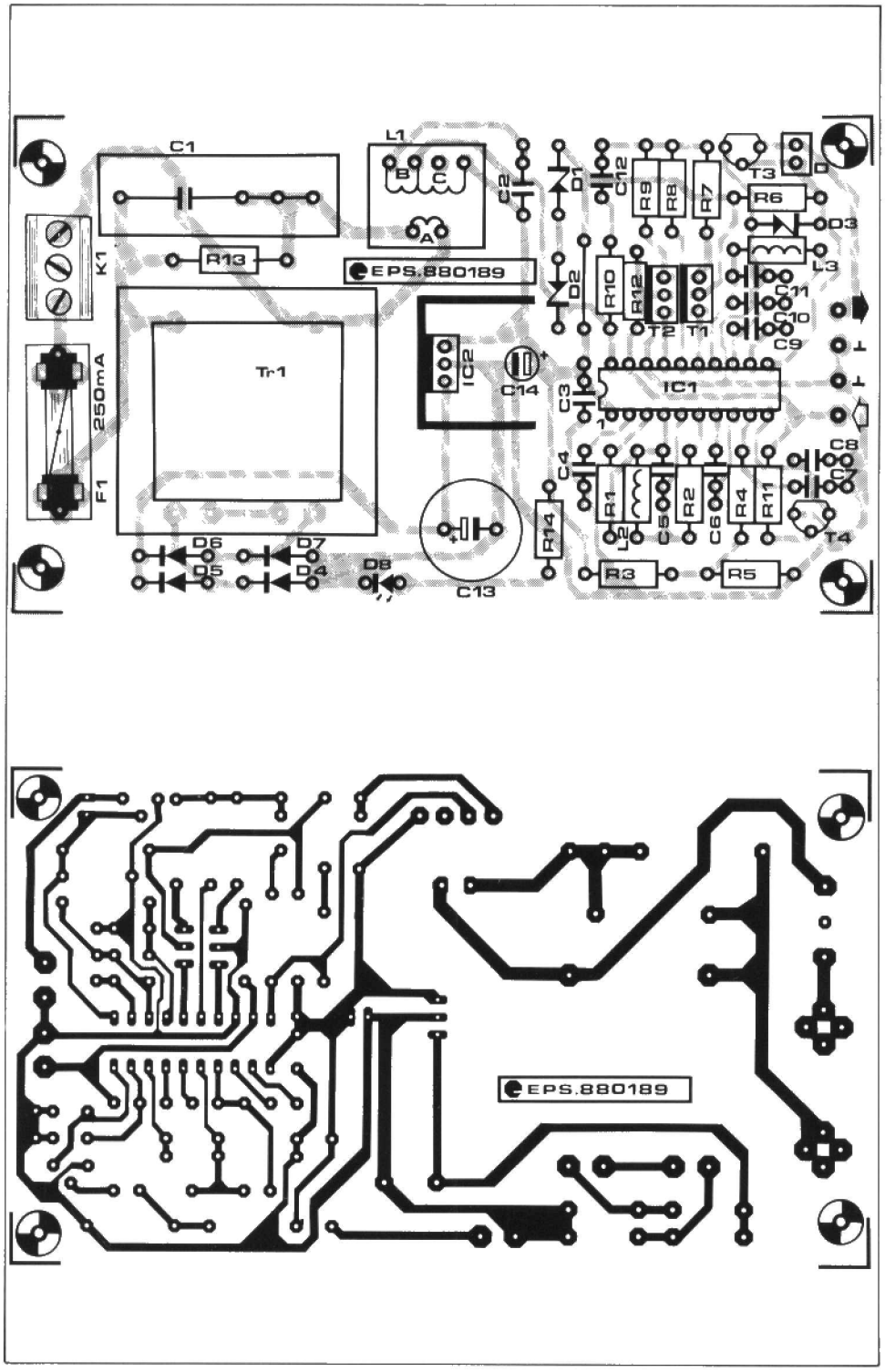


Fig. 4. Printed-circuit board for the mains modem.

Parts list

Resistors (±5%):
R1;R2 = 5K6
R3;R13 = 1M0
R4 = 10M
R5 = 220K
R6 = 10K
R7;R9 = 1R0
R8;R12 = 22K
R10 = 10R
R11 = 47K
R14 = 1K0

Capacitors:
C1 = 470n; 630 V
C2 = 6n8
C3;C7;C11 = 100n
C4;C5;C6;C10 = 4n7
C8 = 10n
C9 = 27p
C12 = 1μ0
C13 = 1000μ; 40 V; radial
C14 = 1μ0; 16 V; radial

Semiconductors:
D1;D2 = BZT03C15+ (Philips Components)
D3 = 5V6; 400 mW zener diode
D4 . . . D7 incl. = 1N4001
D8 = red LED
T1 = BDX77+
T2 = BDX78+
T3;T4 = BC547B
IC1 = NE5050+ (Philips Components)
IC2 = 7812

+ Listed by Universal Semiconductor Devices Ltd.

Miscellaneous:
L1 = VAC ZKB 490/255 (VAC Vacuumschmelze GmbH • Werk Hanau • Grüner Weg 37 • 6450 Hanau 1 • West-Germany. Tel. +49 6181 362-1; telex 4184863; fax +49 6181 362645).
L2;L3 = 390μH
S1 = double-pole on/off switch.
F1 = 250 mA delayed action fuse with PCB-mount holder.
Tr1 = PCB mount transformer; 3 VA; 2×7.5 V @ 200 mA.
K1 = 3-way PCB-mount terminal block.
Heat-sink for IC2.
Moulded ABS enclosure, e.g. Bopla E440, or OKW A9030065.
PCB Type 880189 (see Readers Services page).

other modems, but also its own transmitted signal. In the present application, the receiver is, however, disabled while the modem is in transmit mode. This is achieved by having the transmit input drive T4. When this is turned on, it pulls the comparator output, pin 10, low, so that the bistable can not change state. When the data input line is low, no carrier is transmitted.

The received signal is first applied to an amplifier provided with a band-pass characteristic. The high-frequency roll-off point is internally set to 300 kHz. Dimensioning C4 allows defining the lower roll-off point in accordance wit the carrier frequency used. To ensure selectivity at the carrier frequency, a band-filter, L2-C5, is inserted between the input amplifier and the detector. C6 and components internal to the detector create a low-pass filter for shaping and cleaning the digital pulses. This filter not only suppresses high-frequency signals, but also sets the maximum data rate — in this case, to 1 Kbit/s. Background signals at the mains frequency are rejected by the AM-suppressor. This works by storage of the average direct voltage level in C7. When no input signal is available for more than 4 s, the voltage on C7 would rise slowly to a value that results in a logic high level at the output. This is prevented by R3, R4 and R5.

The comparator, in combination with C8, cleans the detected pulses, whose edges are straightened again by the inter-

Table 1.

Interface configuration options

Component	TTL	HOMENET	RS-232
D3	1	0	0
T3	0	1	0
J1	1	0	1

1 = fit component
1 = omit component

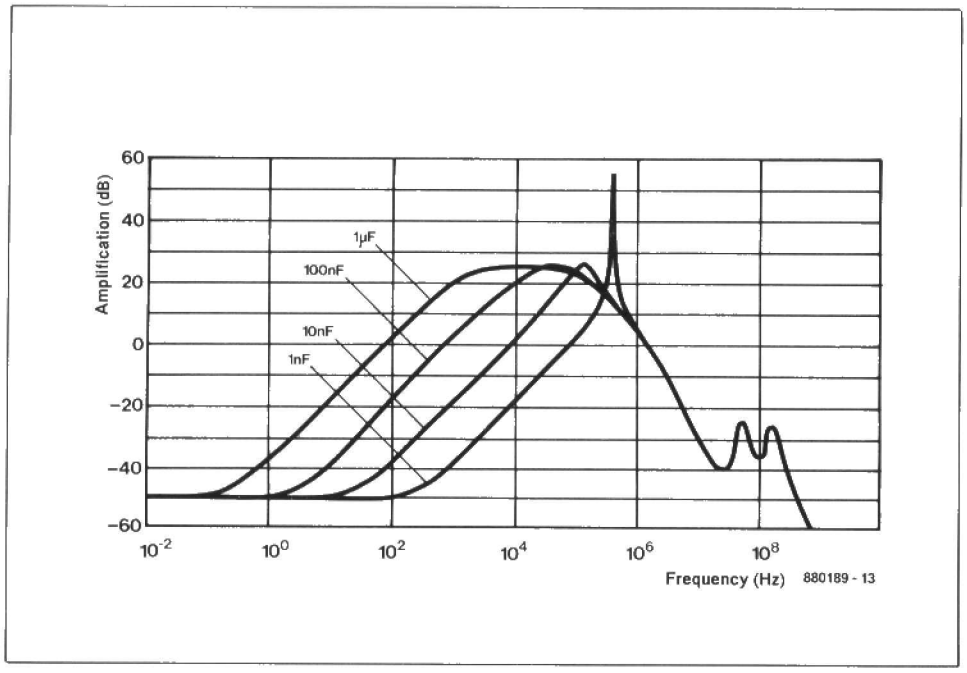


Fig. 5. Receiver amplifier gain vs frequency for different values of the high-pass capacitor.

nal bistable. This has an open-collector output that drives a simple computer interface set up around T_3. Table 1 lists the possibilities of configuring this interface in accordance with three interfacing standards. Since an RS-232 interface works with positive and negative voltage levels, the interface should be extended as shown in Fig. 3. R_{15} and R_{16} simply raise the ground potential of the interface to half the supply voltage of the modem. This results in the circuit driving the RS-232 interface in the computer with a voltage swing of ±6 V, which is adequate for correct operation in most cases. Ground of the circuit is, therefore, **not** ground of the RS-232 interface. One additional resistor, R_{17}, is needed to protect the data input of the modem against the voltage levels of up to ±12 V supplied by the computer's RS-232 driver.

Noise suppression by the modem can be improved by increasing the value of C_6 and C_8 to 10 nF and 100 nF respectively. This measure effectively results in a lower bit-rate of 300 per second, but speed up communication between modems since less information needs to be sent back and forth on account of corrupted data. Finally, some experimenting may be required with the value of C_4 — a lower value results in a narrower bandwidth of the input amplifier. Possible capacitor values lie between 470 pF and 1 nF.

Construction: safety first

For your own safety, the power line modem must never be constructed on a printed circuit board other than the one shown in Fig. 4.
Completion of the board with reference to the parts list is not expected to cause difficulty. The unit is fitted in an ABS enclosure provide with a grommet and a strain-relief clamp for the mains cord. The connector or socket for the bidirectional serial link to the computer should be located as close as possible to the rfelevant connections on the printed circuit board, so that the wires can be kept as short as possible.

One adjustment

To begin with, the data input of the modem should be held at about +5 V. This is easiest done by connecting a 27 kΩ resistor between the input and the +12 V line in the modem. Never apply power until a thorough check of the completed board, and the way it is connected to the mains, has been made.
Power up and use an oscilloscope to inspect the waveform at pin 20 of IC_1. Adjust the core in L_1 for maximum amplitude of the carrier. When an oscilloscope is not available, an analogue voltmeter may be used instead, but only if this is known to be able to work at 120 kHz in the alternating voltage range.

Sending and resending packets: enter Kermit

As already hinted at, reliable data communication with the modem can only be achieved when the computers at both ends run a communications program capable of error detection and correction. Owners of the Commodore C64 computer are advised to use General Electric's excellent program HOMENET.
The prototype of the power line modem was tested under control of the PC communications package PROCOMM version 2.4.2, whose capabilities are outstanding considering the cost. PROCOMM is set to the Kermit mode with the following line settings (ALT-P; option 7): 8 data bits; 1 stop bit, no parity; 300 baud; half-duplex and a time-out of 999 ms. In Kermit mode, PROCOMM allows the user to define the packet size. Initially, go to the Kermit setup menu, and select a small packet size to keep resending time low.
The Kermit protocol works basically as follows. The first packet sent by the computer is accompanied by a CRC byte (CRC = *cyclic redundancy check*). The CRC byte generally provides better results than a *checksum* by virtue of a different method of calculation: the checksum is obtained by addition, the CRC by division. After reception of the data in the remote computer, the CRC is checked, and a message is returned to indicate whether or not the packet has to be resent. This process is repeated, if necessary, until correct data has been received.

Once the maximum feasible parameters for data communication with the aid of the Kermit protocol are known with both modem stations, the chat mode in PROCOMM can be selected for on-line communication between connected PC stations. ■

HOMENET is a registered trademark of the General Electric Corporation. The HOMENET communications package for C64 computers may be obtained by contacting The Industry Standards Staff, General Electric Corporation, Fairfield CT 06431, U.S.A. Reference: Philips Components AN1951.

Procomm is a registered trademark of Datastorm Technologies Inc., P.O. box 1471, Columbia MO 65205, U.S.A. The latest version of Procomm is stated to cost US $35.00 including disk. Datastorm's auto-answer BBS service can be contacted 24 hours a day and 7 days a week on telephone number USA 314 449-9401.

Note: in Philips Components' *Application Note AN1951* on the NE5050, a line transformer identified as TOKO AMERICA #707VX-T1002N is recommended for 110 V mains networks.

Readers are advised that Mains Signalling in the UK is subject to the provisions of British Standards BS6839. Further information on the subject may be obtained from BIMSA (BEAMA Interactive and Mains Systems Association), Leicester House, 8 Leicester Street, LONDON WC2H 7BN, telephone 01-437 0678.

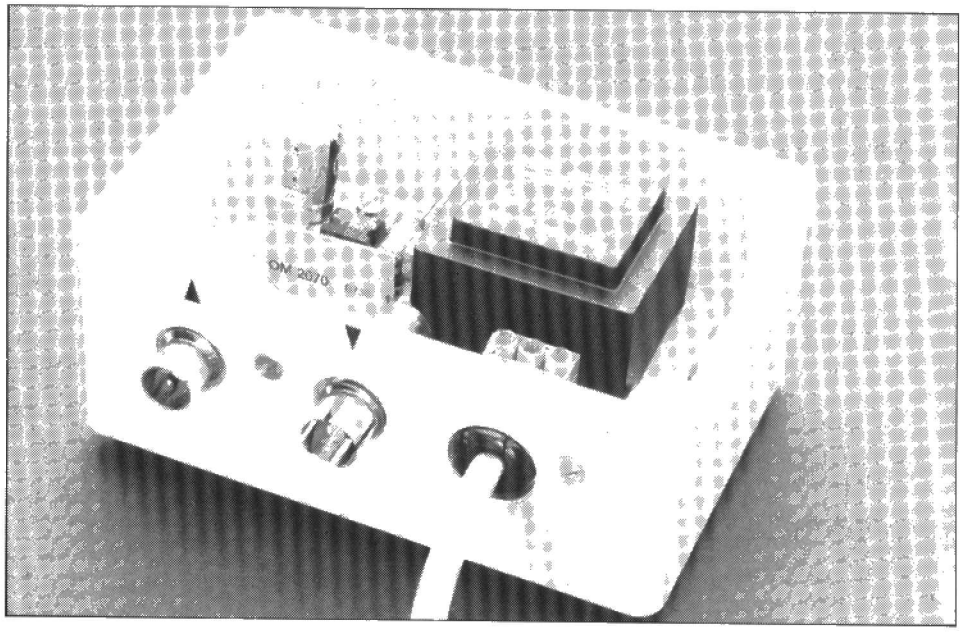
HYBRID VHF/UHF WIDEBAND AMPLIFIERS

Recently, Philips Components have added a number of new devices to their well-established OM3xx and OM9xx ranges of hybrid wideband amplifiers made in thick-film technology. The five new integrated circuits provide a wide range of gains, and should be of particular interest for the design of VHF/UHF wideband boosters, since they require remarkably few additional components. A fully worked out application of the new chips in such a booster is included in this article.

by H. Stenhouse

The new devices in Philips Components' series of integrated wideband amplifiers include a single-stage type, the OM2045 with a gain of 12 dB, a two-stage type, the OM2050 with a gain of 18 dB; and two three-stage types, the OM2060 and OM2061, with gains of 23 dB and 28 dB, respectively. All of these can be used as RF gain blocks with an input and output impedance of 75 Ω, in the frequency range between 40 and 860 MHz.

Since virtually all that is necessary for building a reliable wideband RF amplifier with good specifications is contained in a single chip, many applications are feasible. The amplifiers are, for instance, ideal for use in the domestic cable network for radio and TV, in which additional gain is often required to overcome cable losses. Radio amateurs, too, will find the amplifiers useful for general-coverage reception experiments, as the 6-m band, 2-m band and 70-cm are covered in one go. One further application is the use in 480 MHz or 612 MHz intermediate-frequency (IF) amplifiers of indoor units for satellite TV reception which incorporate a surface-acoustic wave (SAW) filter with high insertion loss.



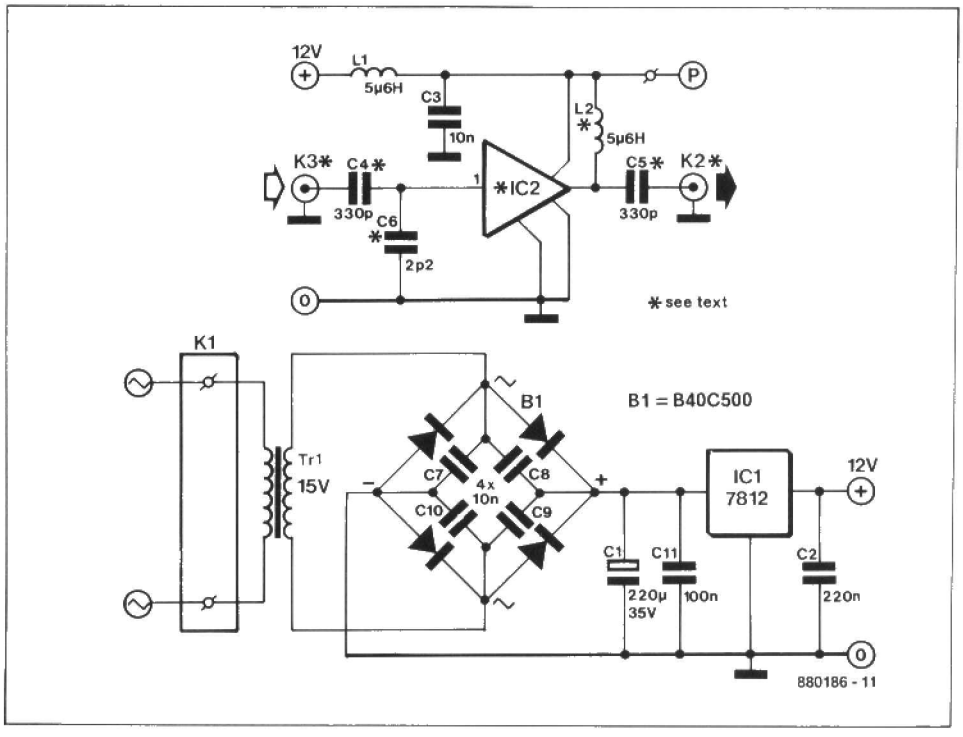


Fig. 1. Circuit diagram of the wideband aerial booster based on Philips Components' latest types in a series of hybrid amplifiers.

A practical design

The circuit diagram of Fig. 1 demonstrates the simplicity of a VHF/UHF wideband amplifier set up around one of the new OM20xx types. Apart from a supply and, of course, the hybrid chip, all that is needed to obtain a complete RF amplifier are two capacitors and a small choke if a two- or three-stage amplifier chip is used. Thanks to the simplicity of the circuit, it can be housed in a compact enclosure. The supply voltage for all amplifier chips is 12 V ±10% at a maximum current drain of 110 mA (OM2070), allowing the use of a simple power supply composed of a small 15 V mains transformer, a 500 mA bridge rectifier, a

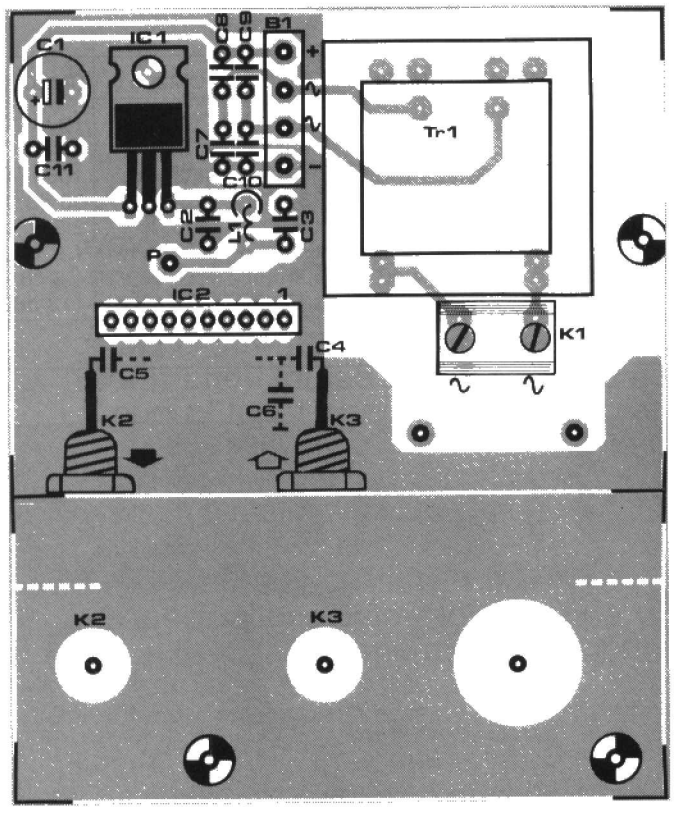


Fig. 2. Component mounting plan of the double-sided printed circuit board.

Parts list

Capacitors:
C1 = 220μ; 35 V
C2 = 220n
C3 = 10n ceramic
C4;C5 = 330p
C6 = 2p2
C7 to C11 incl. = 100n

Inductors:
L1 = 5μH6
L2 = 5μH6 (see text)

Semiconductors:
B1 = B40C500 bridge rectifier (rectangular type)
IC1 = 7812
IC2 = see text

Miscellaneous:
Tr1 = mains transformer 15 V; 50-200 mA (see text).
K1 = 2-way terminal block for PCB mounting.
K2;K3 = TV coax socket.
PCB Type 880186 (not available ready-made through the Readers Services).

220 μF smoothing capacitor and a 7812 integrated voltage regulator with the two usual decoupling capacitors.

Construction of the RF amplifier

The printed-circuit board shown in Fig. 2 was designed to make construction of the wideband amplifier as simple as possible, while still allowing the con-

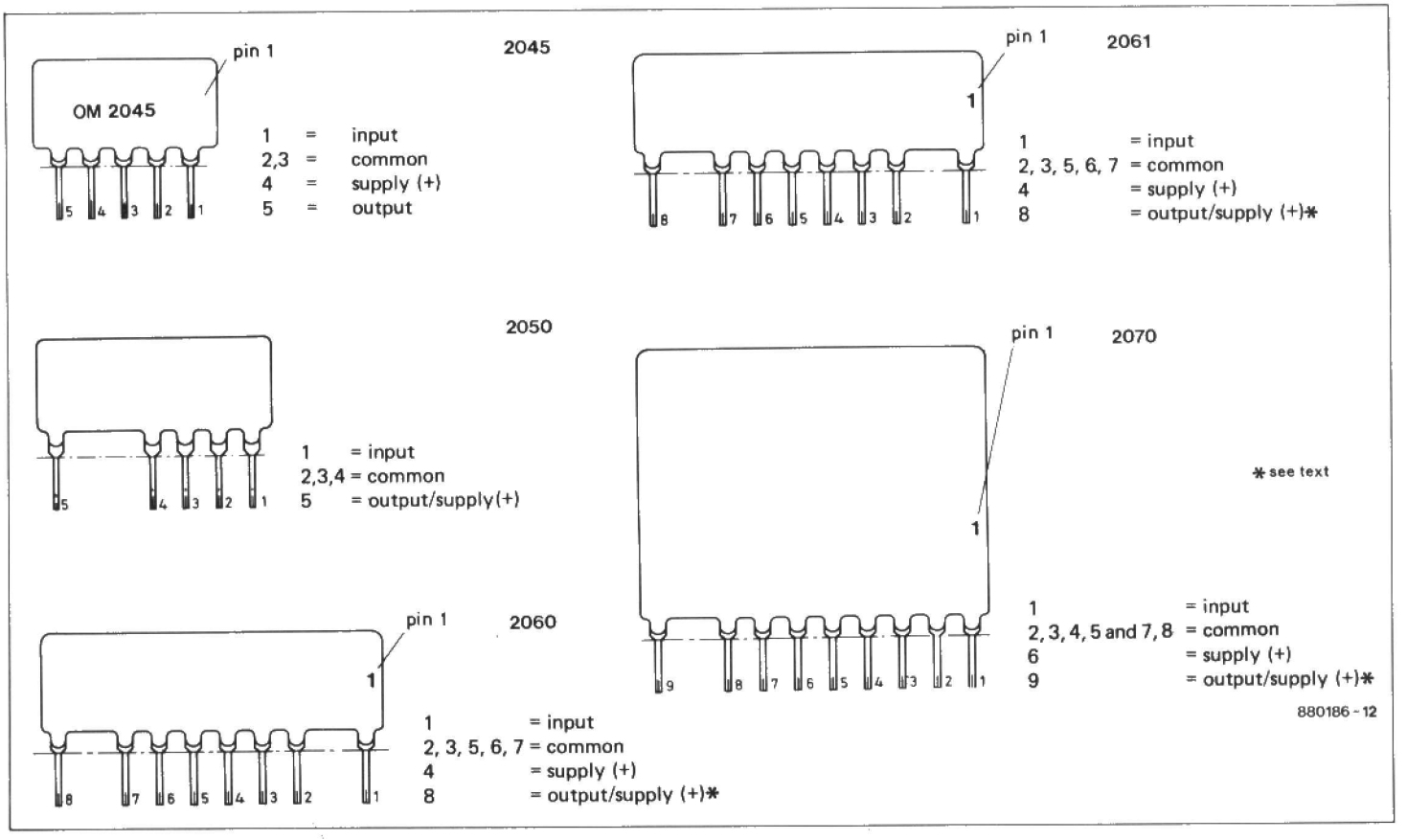


Fig. 3. Pinning of the new hybrid amplifier chips.

structor to choose and use any of the five new amplifier chips. Since the pinning of these is, unfortunately, not consistent (see Fig. 3), short wires are used instead of PCB tracks to connect input, output and supply terminals. In view of the relatively high frequencies involved, it is imperative that these wires, notably the earth connections, are not longer than 1 to 2 mm. In all cases, reference should be made to Fig. 3 to ascertain the pinning of the selected chip.

The power rating of the 15 V transformer on the PCB should be in accordance with the RF amplifier chip used — see Table 1 for the main specifications of these. When the OM2045 is used, a 1.2 VA transformer should do. The use of the OM2070, however, calls for a type rated at not less than 3.3 VA. It should be noted that some transformers require two short pieces of wire between the secondary terminals and the tracks leading to the AC connections of the bridge rectifier.

The PCB is cut in two along the dashed lines. The part with the round, etched, holes is drilled to accept the input and output sockets, and the grommet for the mains cable. After drilling, this part of the PCB is soldered vertically on to the main amplifier board as shown in the photographs. Small pieces of tin-plate are bent to shape and soldered round the input and output sockets for additional screening.

The main board may now be populated, with the exception of the amplifier chip, C_4, C_5 and C_6. The centre pin of voltage regulator IC_1 is soldered at both sides of the board.

Ten non-connected solder spots are reserved for IC_2, whose pins are connected with the aid of wires as outlined above. It is recommended to fit these connections at the reverse side of the board. The input marked *supply (+)* is connected to point P. Three ICs, the OM2060, OM2061 and OM2070, require an additional connection between the supply and the chip output. This connection is made in the form of a 5.6 μH choke between the output and point P, as shown in Fig. 4.

Coupling capacitor C_4 takes the RF input signal direct from socket K_3 to the input of IC_2. The amplified RF output signal is coupled out to K_2 via C_5. To prevent stray inductance and possible oscillation, the wires of C_4 and C_5 should be kept as short as possible. Capacitor C_6 (2p2) may be added for extra suppression of interference. ◀

Note: the hybrid amplifiers discussed in this article are relatively new components which may not be available everywhere yet. Philips Components (formerly Mullard) distributors in the UK are listed on InfoCard 507 (*Elektor Electronics* April 1987).

Table 1.

Main technical specifications of OM20xx series.

	OM2045	OM2050	OM2060	OM2061	OM2070
U_b	12 V	12 V	12 V	12 V	12 V
$Z_i = Z_o$	75 Ω	75 Ω	75 Ω	75 Ω	75 Ω
I_c (typ.)	11.5 mA	18 mA	55 mA	50 mA	105 mA
Gain	12 dB	18 dB	23 dB	28 dB	28 dB
VSWR in	2.0	1.5	1.3	1.5	2.3
VSWR out	1.4	1.9	1.5	1.7	1.9
F(dB)	3.6 dB	5.2 dB	5.4 dB	4.4 dB	4.8 dB
U_o	99 dBμV	100 dBμV	107 dBμV	107 dBμV	113 dBμV

operating temperature: −20 to +70 °C

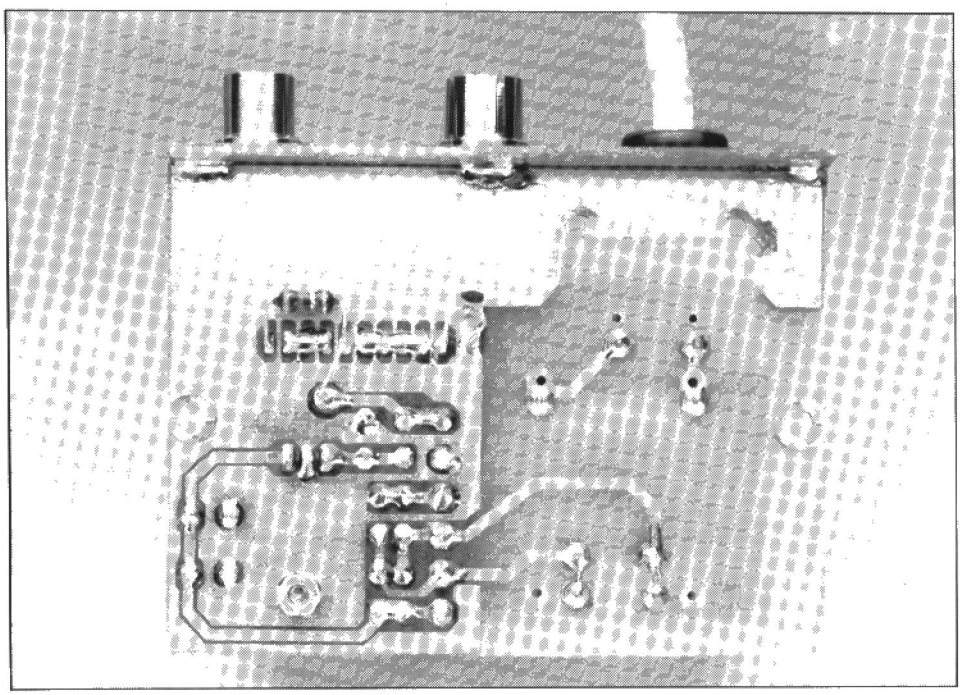


Fig. 4. Series-connected supply choke L_2 is fitted at the reverse side of the board.

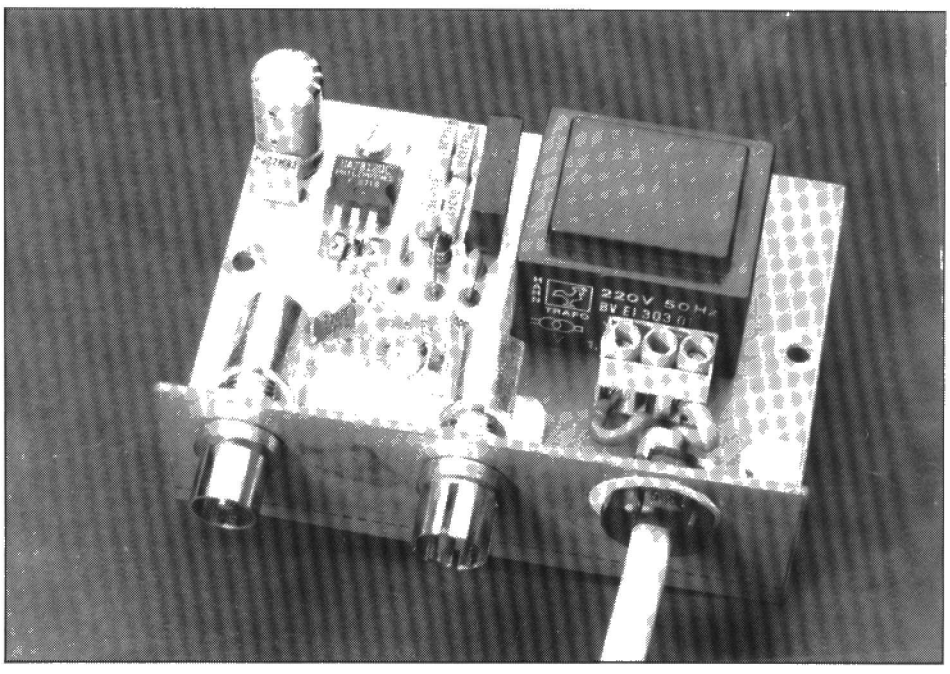
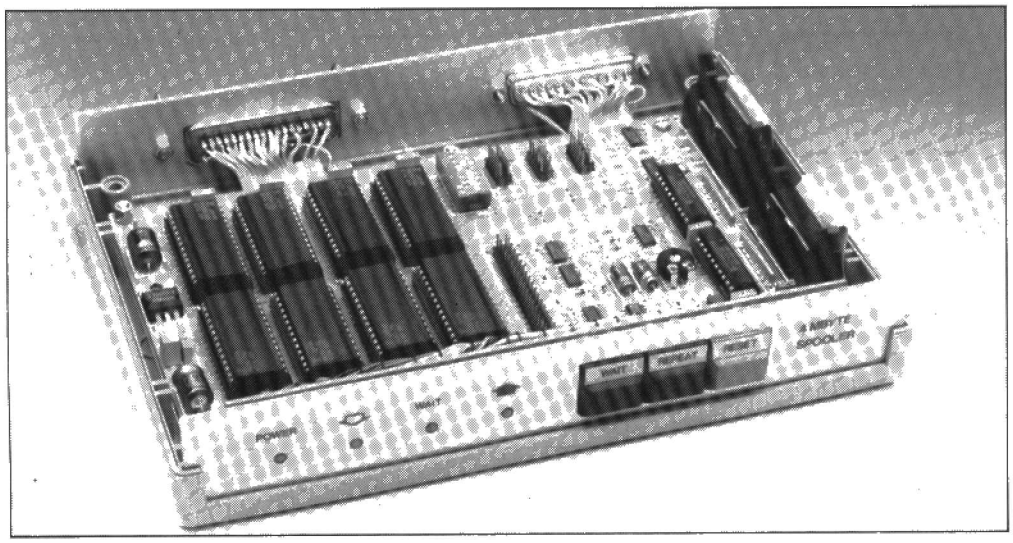


Fig. 5. Completed prototype of the wideband RF amplifier.

CENTRONICS-COMPATIBLE PRINTER BUFFER

from an idea by R. Degen

Today's computers and the programs that run on them are capable of generating massive amounts of data that is, in some way, to be put on paper. Users of computer-assisted design and engineering (CAD/CAE) and desk-top publishing (DTP) programs need not be told that the printer or plotter is almost invariably a slowing-down factor in the system. At printing time, therefore, the user is often forced to sit with his arms crossed, or go out to have a cup of tea, because the computer has insufficient memory left to store the whole of the printable file. Intermediate storage of data on disk and so-called spooler programs only partly resolve this annoying problem.
The versatile printer buffer described here is a state-of-the-art design that eliminates printer wait times. Just look at the main specifications below to convince yourself that this is your next home-made computer peripheral.



Printer wait times arise when the amount of data to be fed to the printer exceeds the free memory capacity of the computer. Today's wordprocessors, CAD/CAM/CAE and DTP programs are so large that, believe it or not, very little memory is left for the work file, be it a text, drawing or graphics image. Often, no more than a few tens of kilobytes are left of the 640 or so installed in the PC. The programs then invariably use a disk drive to temporarily store the excess data, which is 'spooled' to the printer output via the small, internal buffer and a background program. Meanwhile, however, the user can not exit the program, and further text or graphics editing may be slowed down considerably because of the spooling process.
Documentation and other text files are becoming ever larger, too. Many so-called Public Domain programs and PC utilities are accompanied by a compressed documentation file which, when de-compressed (*unpacked* or *uncrunched*) by the user, results in a printable .DOC or .MAN file of 100 kilobyte or so, which takes 15 to 30 minutes to dump on most matrix printers. Most modern matrix and ink-jet printers can be fitted with extra buffer memory, but the cost of such an extension is often quite high relative to the price of the basic printer. The most expensive of add-on buffers often provide 'only' 64 KByte, which is no great help when very large files are handled.

Printer buffer

- Centronics compatible
- Memory: user-configurable from 32 KByte to 1 MByte, or from 128 KByte to 4 Mbyte in six steps. Option to use either 32 KByte or 128 Kbyte static RAM chips (xx256 or xx1024).
- Low current consumption (40 mA) enables powering from printer. Option to use mains adapter with DC output
- Compact unit thanks to surface-mounted components
- No microprocessor
- Repeat mode; buffer does not load data while feeding printer.

A non-used character?

The present circuit is based on the fact that no printer prints ASCII character 00. In practice, the operation of the printer buffer is as follows: the computer writes data into the memory of the printer buffer. When the data flow to the printer buffer ceases, a user-defined delay is introduced before the data lines are made logic low, so that the remaining memory is loaded with zeros (00). The printable file is thus held in the printer

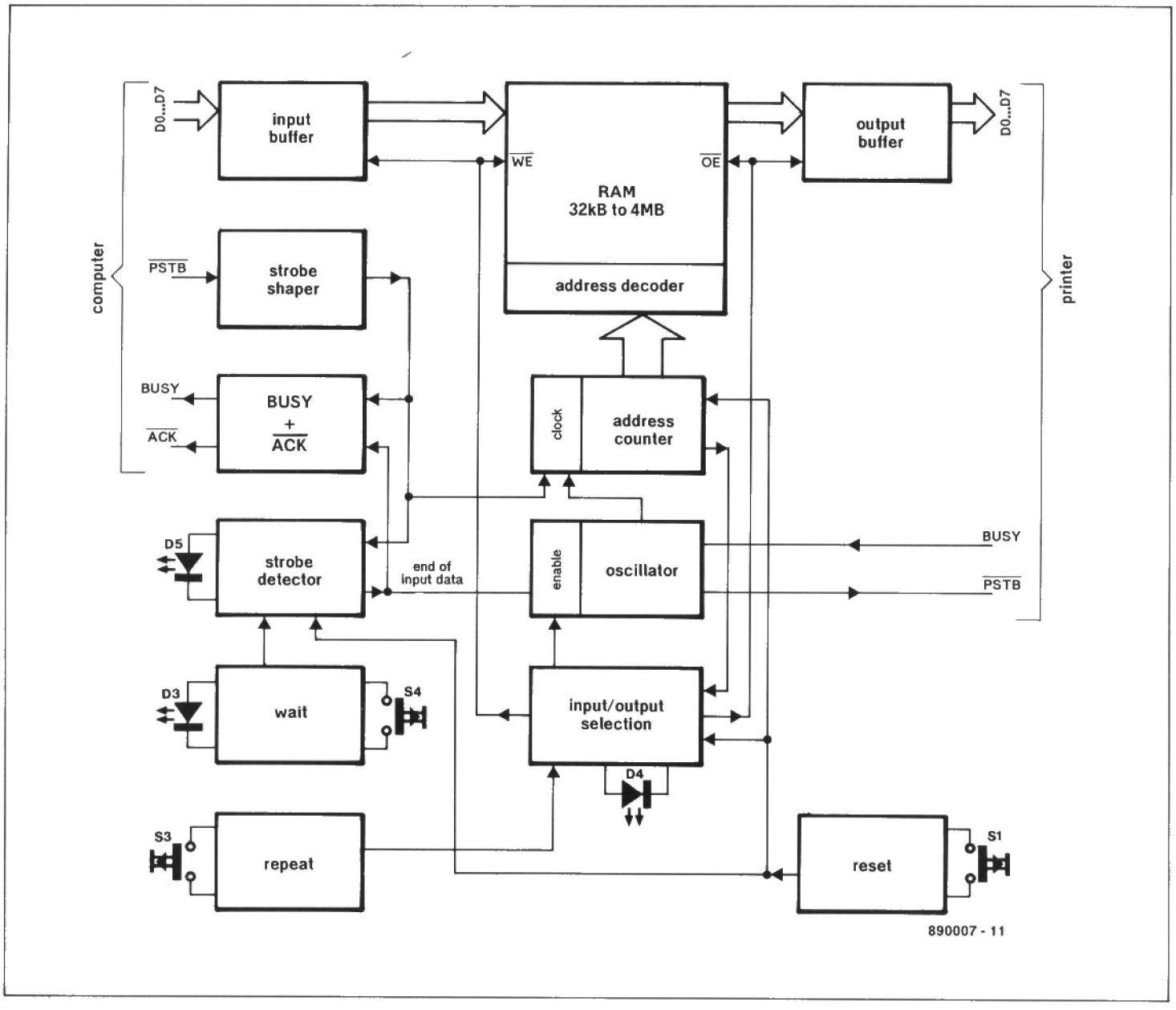


Fig. 1. Basic internal structure of the printer buffer.

buffer, and its size is known. When this process is completed, the file(s) held in the printer buffer are ready for sending to the printer. The total content of the buffer memory, including the zeros, is then fed to the printer (the zeros, of course, do not appear on paper!). The computer is called upon only when the size of the file to be loaded into the printer buffer exceeds the available storage capacity (this depends on the memory configuration selected by the user, and will be reverted to). Provided the computer has not produced a *time-out* error in the mean time, the remainder of the file is loaded after the printer has completed printing the memory content of the buffer.

Obviously, to avoid printable files being loaded in two or more passes, the buffer's memory should have capacity at least equal to the size of the largest anticipated printable file. Few problems are expected here, however, considering that 128 KByte RAMs can be fitted in the circuit. A few examples: the text file for this very article is 29,287 bytes large (WordPerfect 4.2), while the circuit diagram, originally drawn with the aid of OrCad-SDT3, takes up 360 KByte (size A3 sheet). The Postscript DTP file used for composing galley-proofs of this article with the aid of Ventura Publisher 1.2 occupies 422 KBytes. CAD programs, such as PCB design and schematic drawing packages, invariably switch the matrix printer to its graphics mode, and little needs to be said of the 'printing speed' then achieved...

Functional description of the printer buffer

The printer buffer is a relatively complex circuit and it is, therefore, useful to first get acqainted with its general structure, shown in the block diagram of Fig. 1. The function of the keys on the printer buffer is as follows:

WAIT
When several files are to be printed, the printer buffer can be switched to wait mode so that it can load all printable files in succession.

REPEAT
This key enables the buffer to print the same file more than once (copy function).

RESET
The buffer can be reset and re-initialized by pressing RESET. Internal bistables and the memory size counter are reset to zero. It should be noted that reset overrides the repeat function, so that reprintable characters in the buffer may corrupted. The RESET key should not, therefore, be actuated before the buffer has completed feeding out all of the copies selected with the repeat function.

With reference to the block diagram in Fig. 1, the central part is the buffer's memory with its associated address decoding and address counting circuits. The address counter is clocked during the loading as well as feeding out of data. Loading is clocked by the strobe pulses supplied by the computer, and feeding out by an oscillator. At the computer side, an input buffer is provided for the databits, and a clean-up circuit that shapes the strobe pulses and prevents double clocking. A third block takes care of the BUSY and ACK (acknowledge) handshaking with the computer.
The buffer loads and stores data as long as strobe pulses are applied by the computer. The strobe detect block monitors the reception of strobe pulses. When these fail, the oscillator clock is enabled, either to fill the remainder of the internal memory with zeros, or, when the memory is full, to start feeding the printer.
The block marked WAIT FOR INPUT is controlled by WAIT switch S_4 which allows the strobe detect signal to be overridden, thus forcing the buffer to load further data (but only if free memory is still available).
The functions of blocks REPEAT, IN/OUT SELECT and RESET are obvious. IN/OUT SELECT determines the data transfer direction: from computer to buffer (IN), or from buffer to printer (OUT). The databus buffers are required to ensure stable signal levels even when the maximum number of RAMs, 32, is installed.
The BUSY and STROBE signals derived from the previously mentioned oscillator control the data flow between the buffer and the Centronics input of the printer.

The circuit in detail

The above functional blocks are found back fairly easily in the circuit diagram of Fig. 2.
The input handshaking circuit of the printer buffer is composed of IC_{12} and D-type bistables FF_3 and FF_4. Circuits IC_7 and IC_8 form the address counter, and IC_{10}-IC_{11} the address decoder. The memory of the printer buffer is formed by static CMOS RAMs in positions IC_{15} through IC_{22}. Bistable FF_2 and timer IC_9 function as strobe pulse detector that determines when the file(s) has (have) been loaded completely. Direction switching (IN/OUT) as outlined above is effected by bistable FF_1 and Schmitt trigger gates N_{17}, N_{18} and N_{19}.
The central oscillator is an R-C type built around NAND Schmitt-trigger gate N_{16}. Inverters N_{11} and N_{12}, finally, supply the strobe signal for the printer.
The memory extension circuit is shown in Fig. 2b. Each extension card holds 8 RAM chips, which are either 32 or 128 KByte types. The extension(s) is/are essentially connected in parallel to the basic memory on the main board.

Timing is essential

The letters shown at a number of essential points in the circuit diagram refer to the timing diagram of Fig. 3.
Bistable FF_3 slightly lengthens the strobe signal, A, which is supplied by the computer's Centronics port, so that a well-defined rectangular signal, B, is obtained for driving gate N_{20}. This supplies the computer with handshaking signals BUSY (C) and, via N_8 and FF_4, $\overline{ACK}$ (D). Note that some computers use BUSY as the handshaking signal, others $\overline{ACK}$, and still others both. The printer buffer is compatible with all of these.

The strobe detection circuit uses a Lin-CMOS (*Linear Complementary Metal Oxide on Silicon*) timer Type TLC555 (IC_9) from Texas Instruments. The first strobe pulse from the computer triggers the TLC555, which drives its Q output logic high. This causes the output of inverter N_5 to go low (signal G), so that the data reception indicator, LED D_5, lights. When the strobe pulses cease, timing capacitor C_5 is charged via R_7 and preset P_1, which allows setting a delay between 5 and about 30 s. When this delay has lapsed, the voltage on C_5 resets the TLC555. As long as strobe pulses are being received, however, C_5 is discharged by T_1, so that IC_9 can not be reset.
The rising edge of signal G clocks bistable FF_2. Since the D (data-) input of FF_2 is logic high, output $\overline{Q}$ goes low. This results in the output of N_{19} going logic high (signal H). The event marks the switching over from IN (computer to buffer) to OUT (buffer to printer), and at the same time causes the BUSY line to the computer to be actuated.

After a short delay introduced by R_{12}-C_7, the oscillator around N_{16} is started. The memory space available after loading the file(s) is then filled with zeros by disabling the data input latch, IC_{12}, and pulling the datalines to the RAMs to ground with the aid of 8-way resistor network R_{18}.
When the address line selected with RAM-configuration switch block S_2 goes logic high, the outputs of FF_1 toggle. Functionally, this means that the RAM is switched over from read to write ($\overline{WE}$, signal N, is actuated). Via N_1 and N_{13}, the clocking of FF_1 also causes the address counter to be reset in preparation for the feed-out operation.

Signal P controls gate N_{18}, and so enables the communication with the printer to be established. Gates N_{18} and inverters N_{11}-N_{12} convert the oscillator pulses to strobe pulses ($\overline{PSTB}$; signal R) for the printer, which responds to them by actuating output line BUSY (signal Q). This stops the oscillator while a character is printed. When BUSY is de-actuated, a new strobe pulse is generated.
Components R_{16} and C_9 delay the strobe signal briefly with respect to the selection signal, F, for the address decoding circuit. This is done to ensure that the datalines are stable when the strobe line goes low.
The next clock pulse applied to FF_1 causes this to revert to the start state, and FF_2 to be reset via C_2 and R_6. This brings the circuit back in the initial state.

The second part of the timing diagram illustrates what happens when the printer buffer is fully loaded. Bistable FF_1 takes control of the data-buffers, and switches the circuit to the OUT mode (buffer to printer). Components R_{12} and C_7 ensure correct timing of this operation, preventing loss or corruption of printable data. After printing, D_9 rapidly discharges C_7, and so prevents the oscillator from running on, which would result in the last character being printed a number of times. During this operation, the computer is set to wait when insufficient memory is available. It will be clear that fitting enough memory in the buffer is the best way to avoid this situation.

More details...

The time before the buffer starts feeding data to the printer can be adjusted with P_1 (max. 30 s). The delay can be set in accordance with the type of data sent to the printer. Graphics data, for instance, generally gives rise to a fairly heavy calculation load, so that quite some time may lapse. When the available maximum delay of 30 s is too short, or when a number of separately loaded files are to be printed in rapid succession, the buffer may be set to WAIT mode with the corresponding key. When WAIT is de-actuated, the set delay is introduced again, and printing may recommence.

The RESET key re-initializes the buffer as at power-on. Printing may, of course, also be interrupted at any time by turning the printer off-line (SELECT or ON-LINE key).

Extra copies of the printout may be obtained by pressing the REPEAT key. One proviso here, however, is that the previous run was not interrupted by a reset. This is because the reset circuit works asynchronously and may, therefore, modify the memory content.

Building the printer buffer

The printer buffer is built partly with surface-mount assembly (SMA) parts.

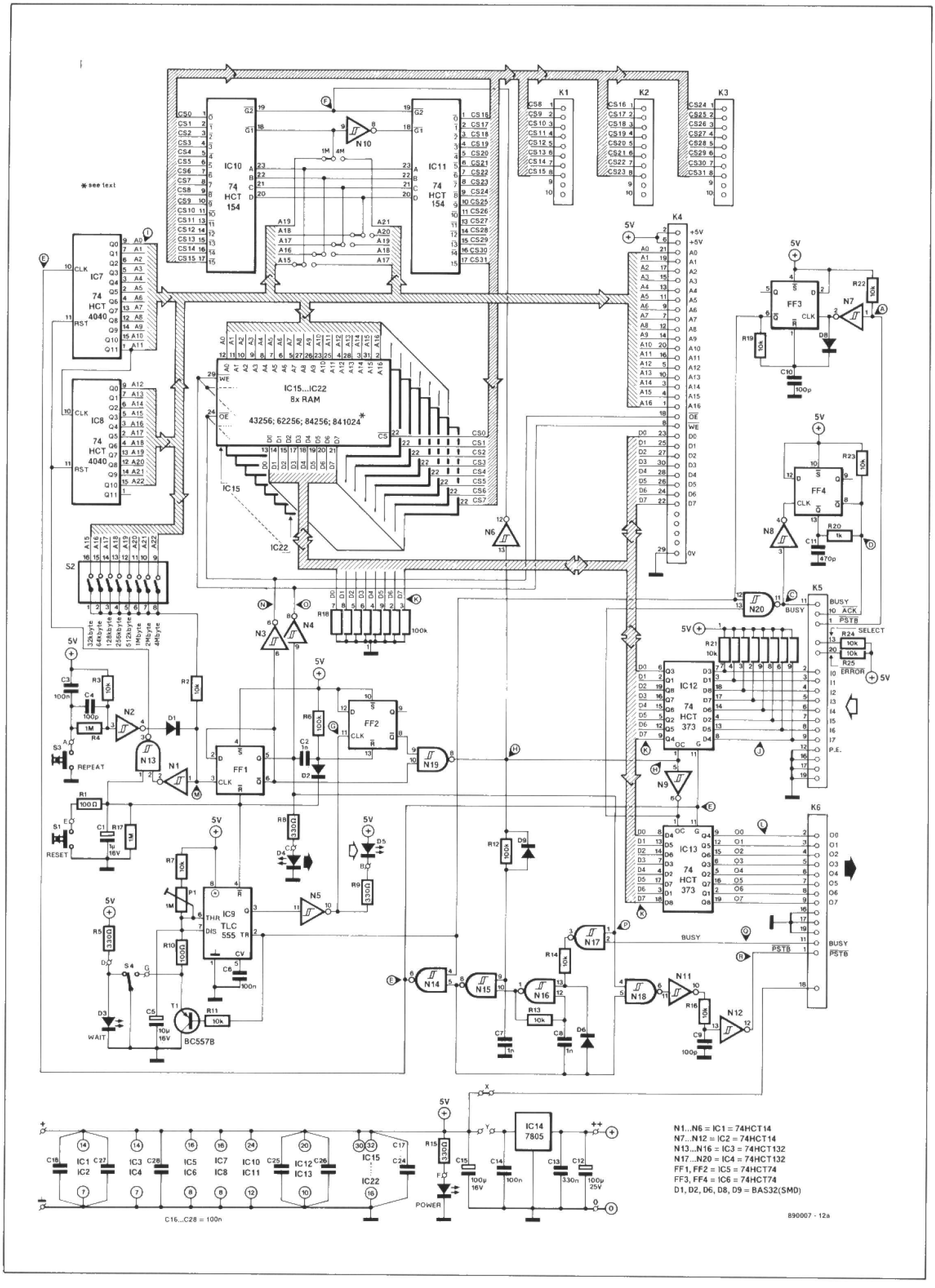


Fig. 2a. Circuit diagram of the printer buffer. The memory configuration is selected by the user.

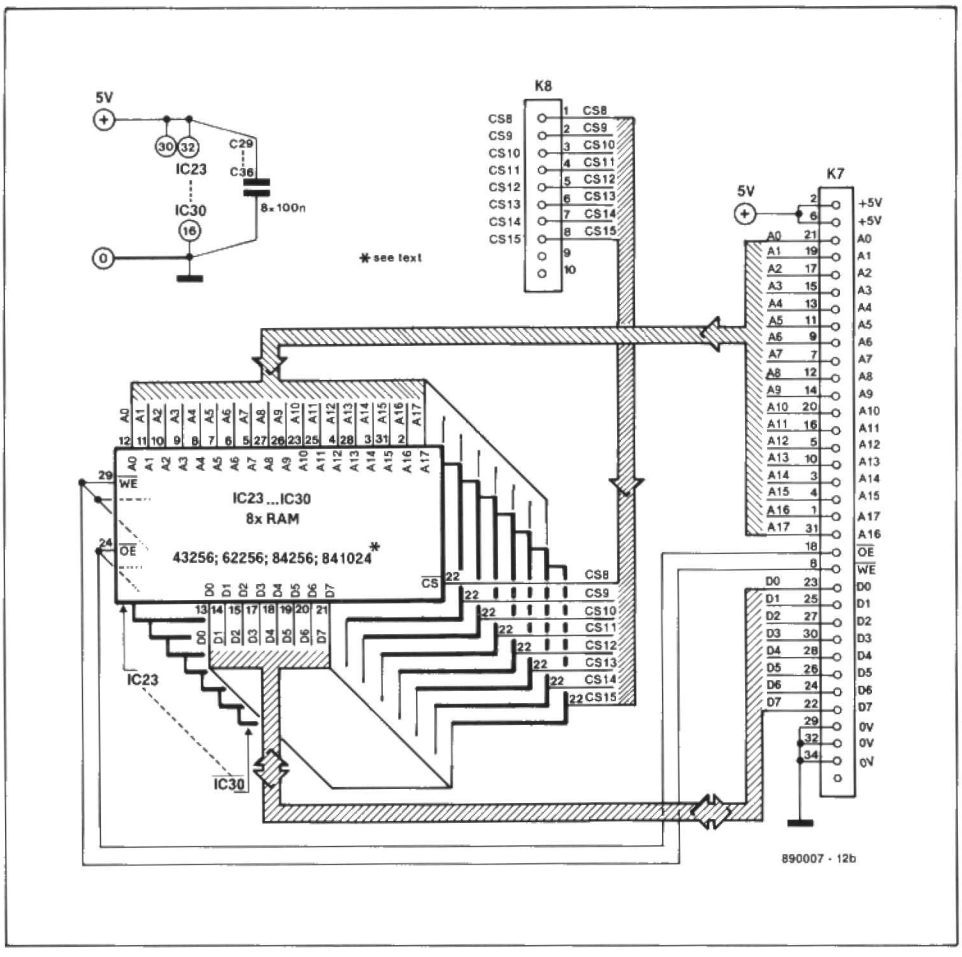


Fig. 2b. Circuit diagram of the optional memory extension board which, depending on the RAM chips fitted, provides 256 KByte or 1 MByte of additional buffer capacity.

The basic circuit is composed of two printed-circuit boards: the main board (Fig. 4a), which holds the digital control and memory circuits, and the keyboard (Fig. 4b), which holds the 3 control keys, and 4 LEDs.

Memory configuration: look before you leap

It was already noted that the user determines the memory size of the printer buffer. A third PCB is, therefore, provided as a memory extension unit (see Fig. 5) that accepts two types of static RAM: 32 KByte (43256 or 84256) or 128 KByte (841024). This third board is only required to increase the memory size of the basic printer buffer beyond 256 Kbyte (32 Kbyte chips used) or 1 MByte (128 KByte chips used.). *Attention:* it is *not* possible to mix 32 KByte and 128 KByte RAM chips. When the memory is to be upgraded, either the first choice must adhered to, or *all* chips must be removed and replaced by other types. On the PCB, there can be no doubt about the location of the chips, since 32 Kbyte and 128-KByte types are supplied in a 28-pin and 32-pin package respectively.

Five short wire links at the copper side of the PCB define the *maximum* size of the memory (either 1 MByte using 32 32 KByte RAMs, or 4 MByte using 32 128 KByte RAMs) — hence, the wire links are marked 1M and 4M. Fit the

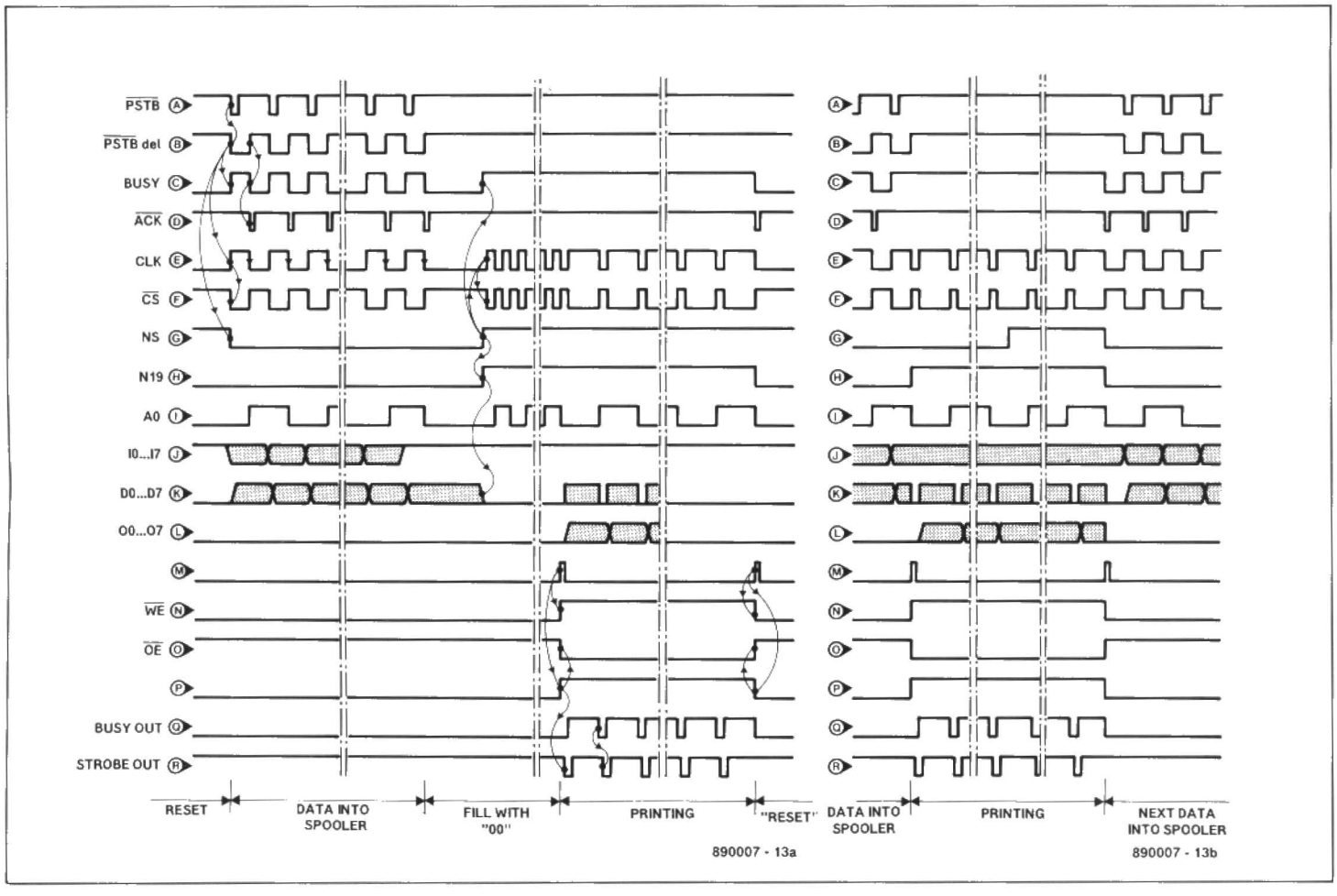


Fig. 3. Timing of the main signals in the circuit.

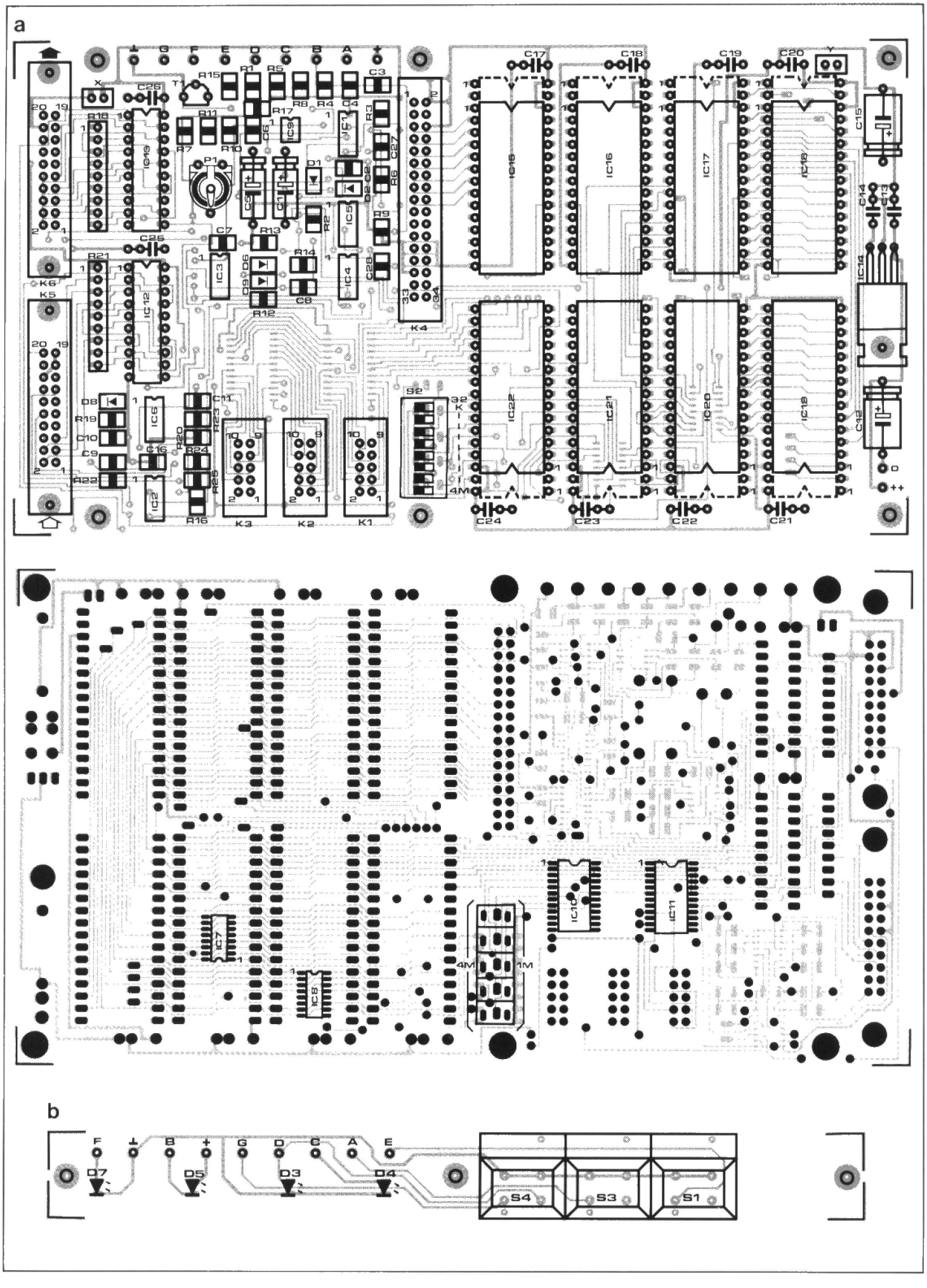


Fig. 4. Component mounting plan of the main board (4a), and the keyboard (4b).

Parts list

PRINTER BUFFER: MAIN BOARD AND KEYBOARD

Resistors (±5%):
R18;R21= 8-way SIL resistor array 10K
P1=1M0 preset H

Capacitors:
C1=1μ0; 16 V
C5=10μ; 16 V
C12=100μ; 25 V
C13=330n
C14;C17 . . . C26 incl.=100n
C15=100μ; 16 V

Semiconductors:
D3;D-f6-4;D5;D7= red LED; 3 mm dia.
T1=BC557B
IC12;IC13=74HCT373
IC14=7805
IC15 . . . IC22 incl.=43256 (NEC) or 62256 or 84256 (Fujitsu) (32K×8)) or 841024 (Fujitsu) (128K×8)

Miscellaneous:
K1;K2;K3= 10-way pin header.
K4= 34-way pin header.
K5;K6= 20-way pin header.
S1= push-to-make button with large black cap (ITW 61-1020400)+ or Digitast.
S2= 8-way DIL-switch block.
S3= push-to-make button with large red cap (ITW 61-1020000)+ or Digitast.
S4= locking button with large black cap (ITW 61-2020400)+.
2 off 20-way IDC sockets.
1 off 36-way Centronics (female) connector for panel mounting.
1 off 25-way female D-connector for panel mounting.
Flat-ribbon cable as required.
Enclosure: e.g. BICC-Vero Type 4775-1410.
PCB Type 890007-1 (see Readers Services page).
PCB Type 890007-2 (see Readers Services page).

+ ITW Switches • Division of ITW Limited • Norway Road, Hillsea • PORTSMOUTH PO3 5HT. Tel.: (0705) 694971. Telex: 86374. Fax: (0705) 666352.

SURFACE-MOUNT ASSEMBLY PARTS:

Resistors:
R1;R10=100R
R2;R3;R7;R11;R13;R14;R16;R19;R22 . . . R25 incl.=10K
R4;R17=1M0
R5;R8;R9;R15=330R
R6;R12=100K
R20=1K0

Capacitors: C2;C7;C8=1n0
C3;C6;C16;C27;C28=100n
C4;C9;C10=100p
C11=470p

Semiconductors:
D1;D2;D6;D8;D9=BAS32 (SMA equivalent of 1N4148)
IC1;IC2=74HCT14
IC3;IC4=74HCT132
IC5;IC6=74HCT74
IC7;IC8=74HCT4040
IC9=TLC555 (Texas Instruments)
IC10;IC11=74HCT154

links marked 1M when xx256 RAMs are used, and the links marked 4M when xx1024 RAMs are used.
A dual-in-line (DIL) switch block, S2, is used for setting the *actual* memory size. Only one switch may be closed at a time: switch 1 selects 32 KByte, switch 2 64 KByte, switch 3 128 KByte, and so on, to S8 which selects 4 MByte. It is seen that each switch doubles the amount of memory, and extending the memory means, therefore, doubling its size (it is not possible to add, say, 32 KByte when 128 KByte is already available: the next step is 256 KByte).

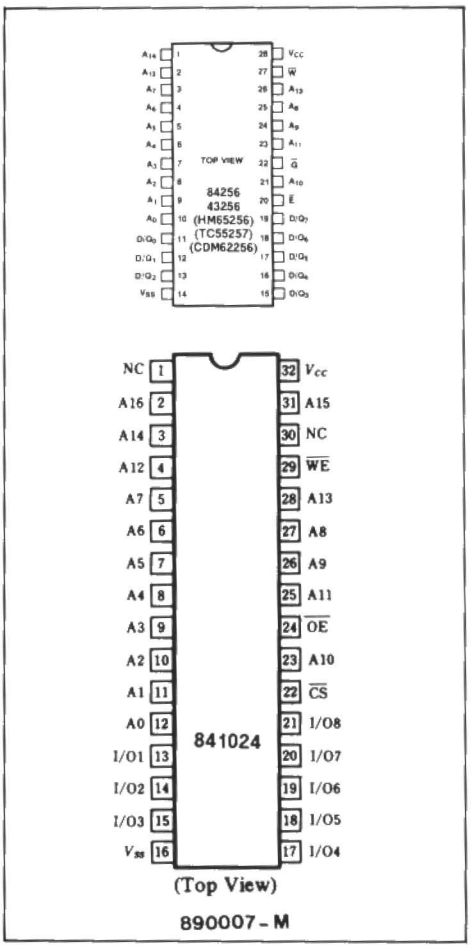
With the cost of the RAM chips in mind, the possibilities for future extensions should always be studied beforehand. For instance, for a 256 KByte configuration, there is a choice between eight 32 KByte and two 128 KByte RAMs. The latter option may currently be the more expensive, but has the advantage of allowing a future upgrade to 1 MByte (on the main board) or 4 MByte (with 3 off 1 MByte extension boards).

Fitting the SMA parts

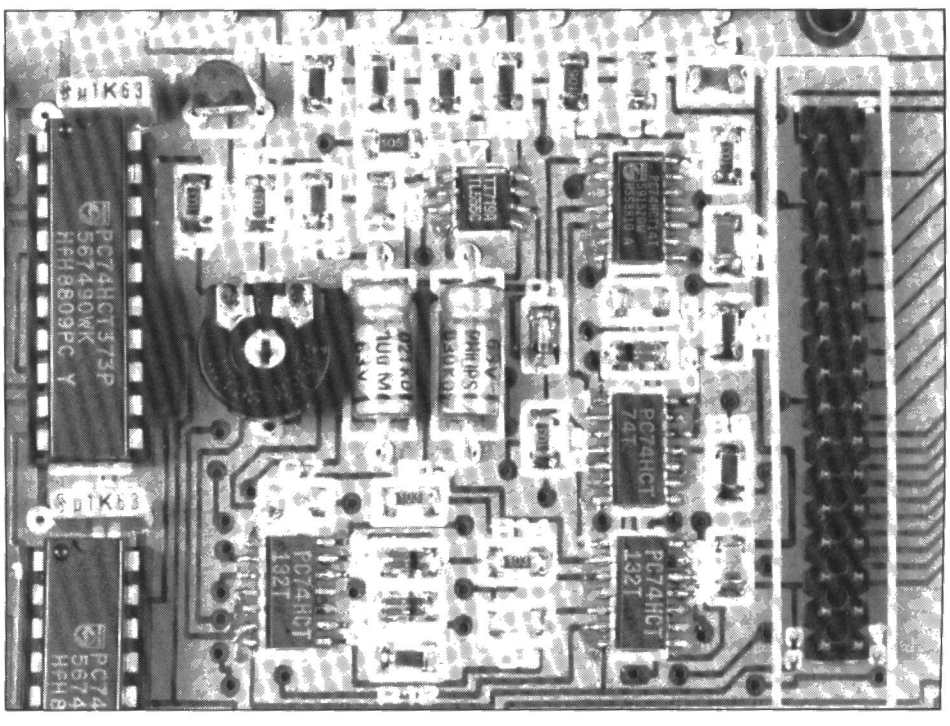
The SMA parts are the first to be mounted at both sides of the main PCB, which is double-sided and through-plated.
There is no mystery about fitting SMA parts if a few basic precautions are observed:

- SMA components generally do not have a printed type or value indication: therefore do not remove them from their labelled package before they are due for mounting;
- use a low-power, temperature-controlled, soldering iron with a fine tip, and clean this after every soldering action;
- use thin (<1 mm dia.) soldering wire to avoid short-circuits between adjacent pins;
- solder as quickly as possible to prevent overheating the component;

SMA integrated circuits should be placed and aligned carefully. Then solder two corner pins and once more



Pinning of static CMOS RAMs Types xx256 and xx1024.



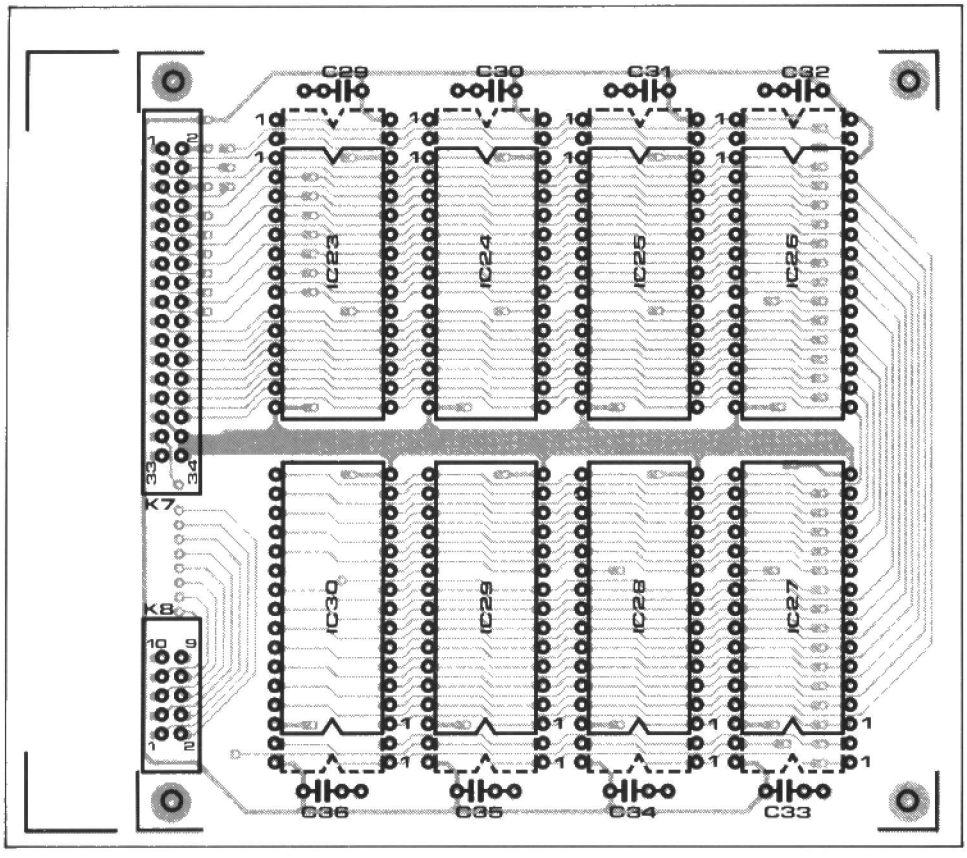


Fig. 5. Component mounting plan of the memory extension board. Depending on the memory configuration, 10-way header K8 is connected to K1, K2 or K3 on the main board.

verify whether all pins line up correctly with the relevant solder islands.
For passive SMA parts, it is best to first pre-tin one of the tracks with a tiny amount of solder. Position the part, and heat the connection on the pre-tinned track. Then solder the other part connection. Again, avoid overheating and excess amounts of solder tin.

When all SMA parts have been fitted, a magnifying glass is used to inspect their connections to the tracks on the board. Also check all solder joints for possible short-circuits.

The standard parts
The first non-SMA part to be fitted is 8-way DIL switch S2. This is mounted as an SMA integrated circuit, slightly above the PCB surface so that its pins are accessible for soldering. If changes in the memory configuration are not foreseen, S2 may be omitted: the connection that selects the relevant RAM size is then made by a wire link. Proceed with fitting the sockets for the integrated circuits, and the memory extension connector(s). The rest of the construction is entirely straightforward.
The memory extension board is not through-plated. With the exception of a number of capacitor leads, the points where through-contacting is effected are, fortunately, located well away from components. Start the construction of this board with fitting the through-contacting wires, as these are difficult to reach once the IC sockets have been mounted. A simple method of through-contacting the PCB is to temporarily insert four M3 screws with nuts in the corners of the board, so that this is a few millimetres above the working surface. Then insert the through-contacting wires vertically until they rest on the work surface. Cut off the excess wire, and solder at the top side. Once all the wires have been fitted, the board may be reversed and the screws removed. The free side of each through-contacting wire is then (quickly) soldered to the relevant spot.

Power supply

The printer buffer may be powered either by the printer or by an internal power supply. Consult the manual supplied with your printer to check whether this supplies +5 V at pin 18 of its Centronics input connector. If this is not so, wire link Y is fitted, and the 5 V regulator circuit on the main PCB is powered from a mains adapter with 8 to 12 VDC output. Wire link Y is omitted, and wire link X is installed, when the buffer is powered from the printer. When the external power supply option is used, it is recommended to connect the mains adapter via a small, 2-way DC-input socket as used on portable cassette players and some older types of pocket calculator.

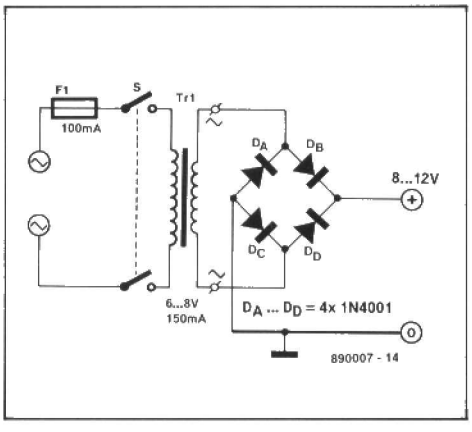


Fig. 6. Build this simple power supply if an 8...12 VDC mains adapter is not available.

Parts list

PRINTER BUFFFER: MEMORY EXTENSION BOARD

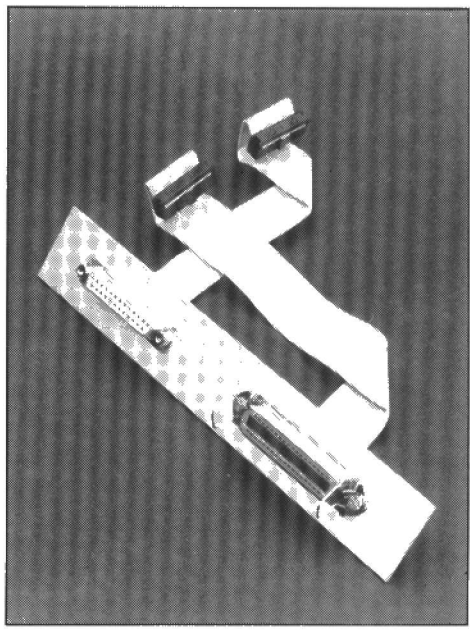
Capacitors:
C29...C36 incl. = 100n

Semiconductors:
IC23...IC30 incl. = 43256 or 84256 or 62256 (32K × 8) or 841024 (256K × 8)

Miscellaneous:
K7 = 34-way angled pin header.
K8 = 10-way angled pin header.
K9;K10 = 34-way IDC socket.
K11;K12 = 10-way IDC socket.
Flat-ribbon cable as required.
PCB Type 890007-3 (see Readers Services page).

Cables and connections

The main board has two 20-way pin headers for connecting the input and output cables. The pin headers mate with 20-way IDC sockets secured on to short lengths of flat ribbon cable. The input cable is fitted with a 36-way Centronics ('blue-ribbon') connector, the output cable with a 25-way D-connector. This arrangement allows the printer buffer to be connected with the aid of a pair of standard, inexpensive, printer cables.



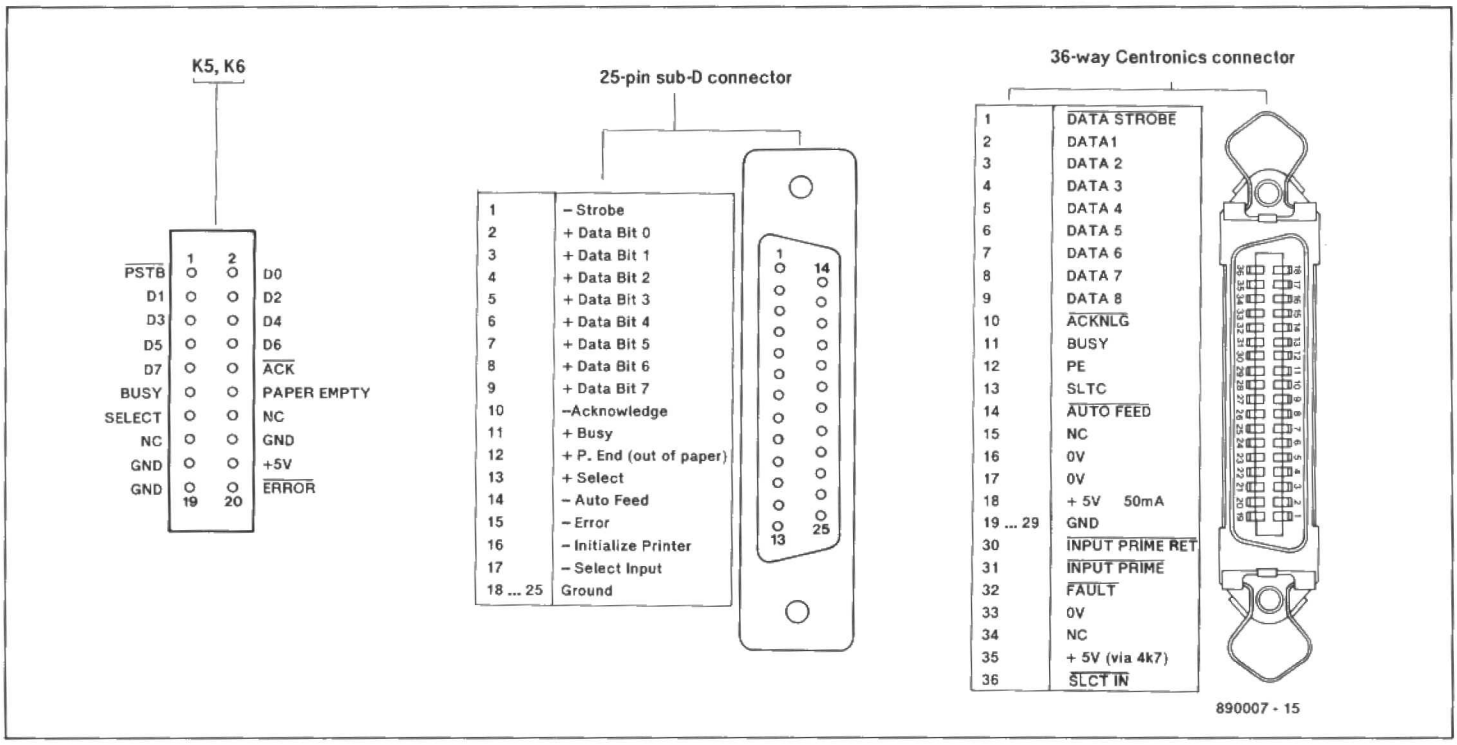


Fig. 7. Pinning of the input/output connectors, K_5 and K_6, on the main buffer, and their wiring to a 36-way Centronics input connector (input) and a 25-way female D-type (output).

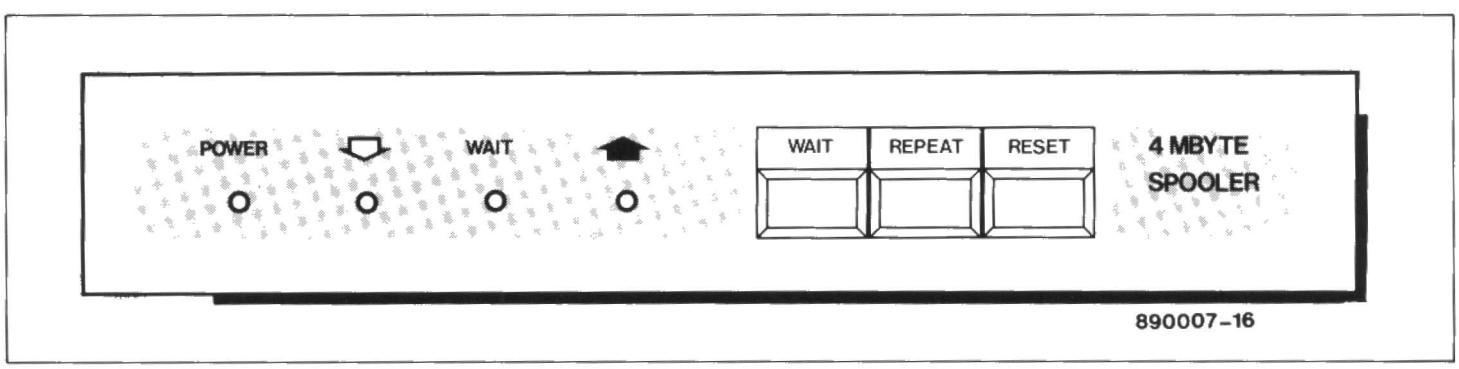
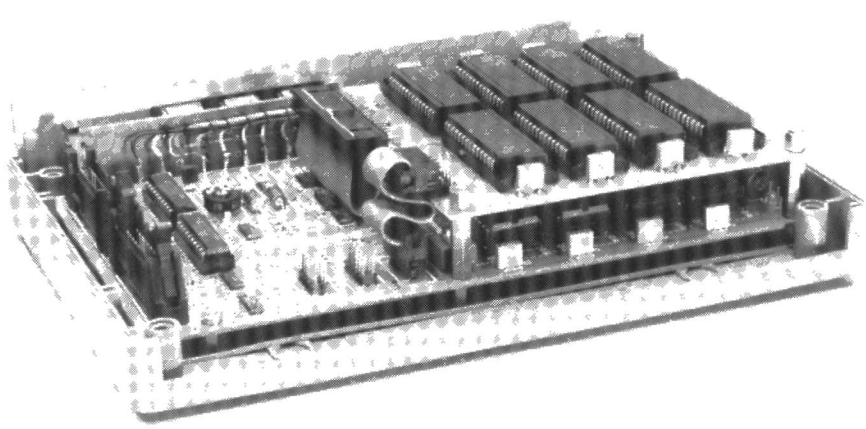


Fig. 8. Suggested lay-out of a front panel for the printer buffer.

Figure 7 shows the wiring diagram of the input and output cables. The pinning of the input and output connectors is identical. On these, the interconections are made as indicated. When a 25-way D-connector is used at the output of the buffer, pin 15 ($\overline{\text{ERROR}}$) may be used to carry the +5 V supply voltage taken from pin 18 of the Centronics connector at the printer side.
The memory extensions are bused and connected to K_4 via a 34-way flat-ribbon cable. Each memory extension board has a 10-way pin header which is then connected to headers K_1 to K_3 on the main board, observing the logic order of the extension boards: the first is connected to K_1, the second to K_2, and the third to K_3.

The control panel, of which a suggested lay-out is given in Fig. 8, is connected to the main board via individual wires. Switch S_4 is a 2-position locking type from ITW.
The size of the control panel is such that it is easily installed vertically behind the



front panel in an ABS enclosure Type 4775-1410 from BICC-Vero. The main board and the control board are mounted on to an aluminium base plate. A drilling template for this support plate is given in Fig. 9.

Test time...

The power LED on the printer buffer should light at full intensity when the unit is switched on. If it does not, the power supply in the printer is not capable of delivering the required current, and a separate power supply should be used as discussed earlier. It should be noted that the printer buffer draws a small current from the computer via the STROBE connection. This current causes the power LED to light dimly.

Once the presence of the correct supply voltage has been ascertained, the WAIT key is pressed. The associated LED should light. Release WAIT.
Send a file to the printer buffer, which shows reception of data by lighting the input LED. After a delay determined by the size of the file, the input LED goes out. The following delay depends on the memory size, and is about 15 s with 256 KByte installed (remember that some time lapses before the non-used part of memory has been filled with zeros). The output LED will now light. Printing commences, and the output LED goes out when the print job is finished. The repeat function may now be tested. When the relevant key is pressed, the associated LED lights, and the buffer should feed out a copy of the previously loaded file. When a number of files are to be loaded for printing in one go, the WAIT key is actuated before the first file is sent to the buffer. Pressing this key remains possible until the file has actually been loaded. The WAIT key is pressed again when the last file in the batch has been sent to the printer buffer.

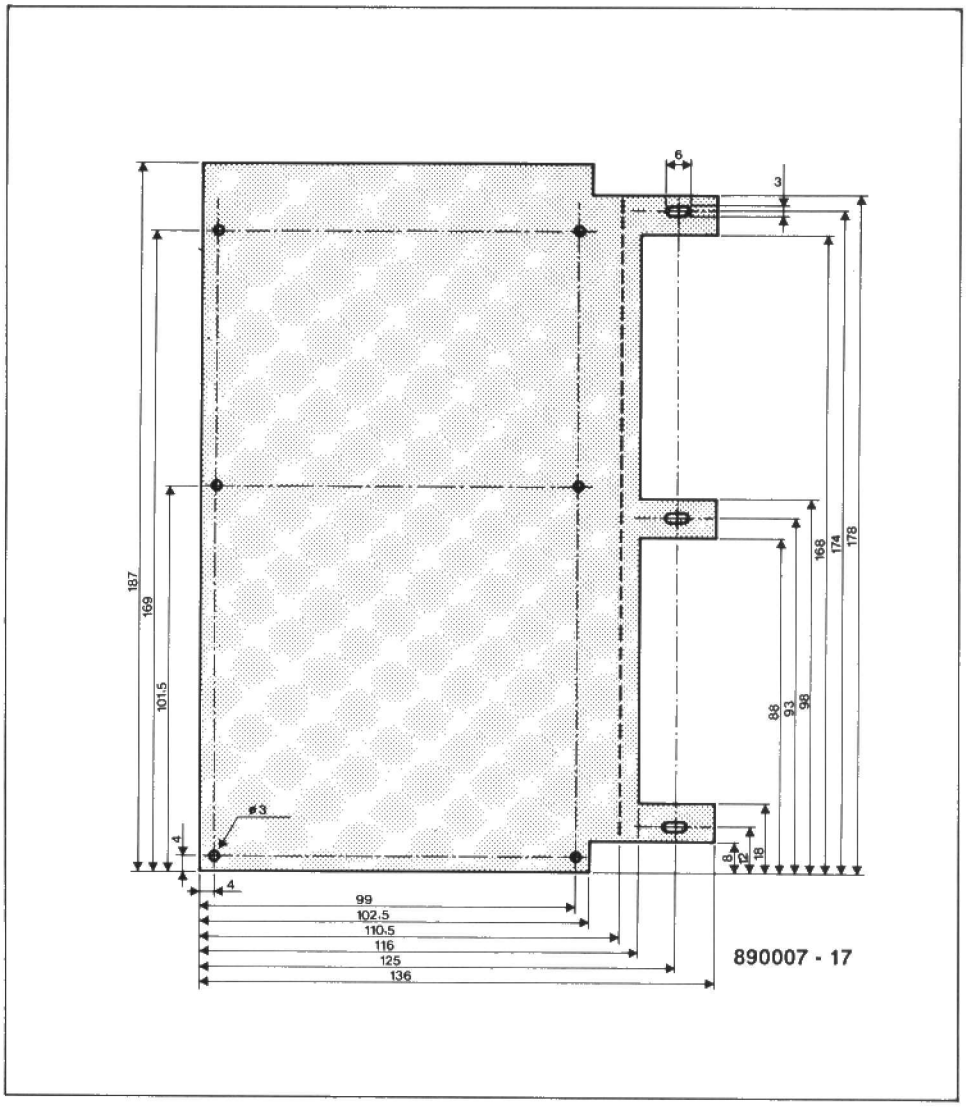


Fig. 9. Drilling template for a support bracket that holds the keyboard.

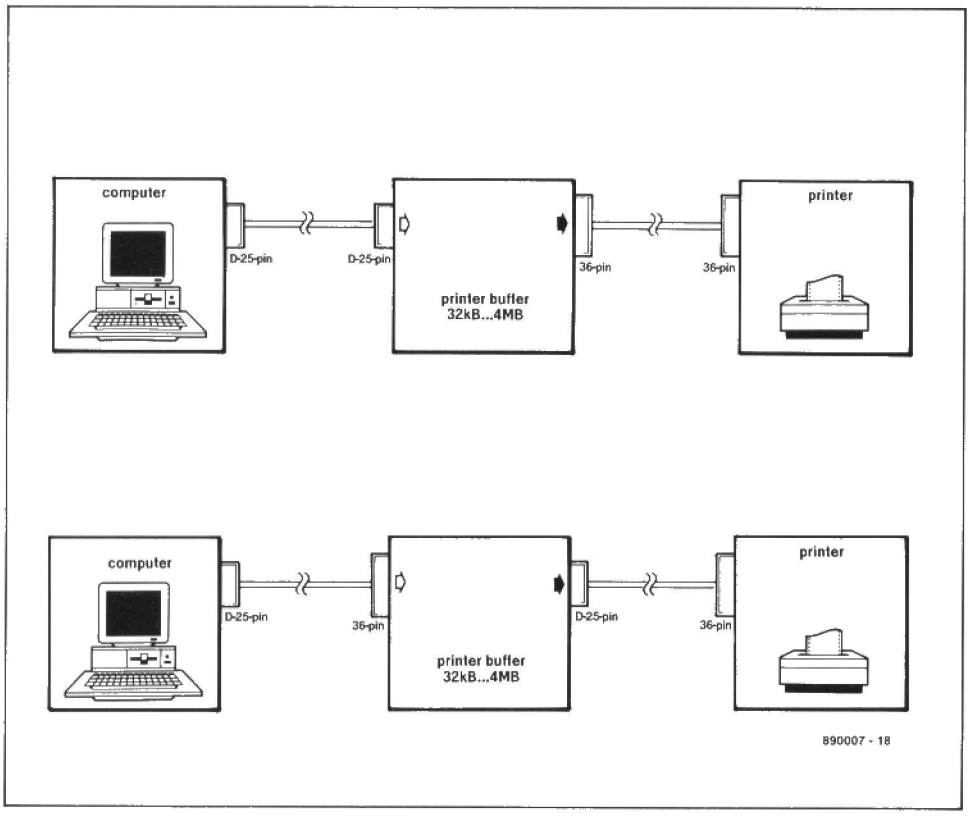


Fig. 10. Examples of how the printer buffer may be connected between the computer and the printer.

The memory configuration switch, S_2, may be replaced by a single wire link if frequent changes in the RAM size are not anticipated. Other options for this switch include an 8-way rotary type, or mounting it on to the rear panel of the printer buffer and connecting it to the main board via a length of flat-ribbon cable and a 16-way DIL header. The rotary switch is a particularly useful arrangement because it allows memory size to be reduced quickly when a relatively small file is to be loaded (because less memory is available, less time is needed to fill the non-used part of it with zeros).

SPECIAL FEATURE: TV AND VIDEO

A look at some recent developments in the TV and video field, with a short introduction to the role of digital picture processing, a technique of great promise for noise reduction and run-time picture enhancement.

Super-VHS: last station before the digital era?

Every owner of a VCR knows that the picture quality of the recording is slightly lower than that of the original programme. Clearly with recent developments in satellite broadcasting in mind, Super (S-) VHS aims at improving the performance of the VCR beyond that offered by VHS.

The most important technical characteristic of S-VHS is the availability of separate inputs and outputs for Y (luminance) and C (chrominance) signals. To ensure downward compatibility of the new S-VHS equipment with existing cameras, VCRs and monitors, CVBS (chrominance; video; blanking; sync) inputs and outputs are also provided.

In the European version of the S-VHS system, the frequency-modulated luminance signal has been shifted from 3.8 MHz to 5.4 MHz, while the deviation bas been increased to 1.6 MHz (see Fig. 1). Separate connection and processing of Y and C signals has resulted in a considerable reduction of cross-talk between luminance and chrominance, and thus affords a marked improvement in picture quality.

The advantages of S-VHS may be summarized as follows:

- Y and C signals are transmitted and received separately in their original form, reducing cross-colour disturbance and dot-interference between the signal components.
- Y signals are recorded at a higher carrier frequency by means of linear sub-emphasis techniques.
- High-performance tapes with 30% higher magnetic coercive force and smoother surface improve the attainable signal-to-noise ratio.
- Luminance resolution is increased from 240 (VHS) to 400 horizontal lines.
- Tape type detection ensures downward compatibility with VHS.
- Hi-fi stereo sound reproduction with a dynamic range of up to 87 dB. Dolby® noise reduction and audio dubbing are often available as options.
- VPS (video programming service) compatible.

It will be clear that the new S-VHS VCRs will only yield optimum results when connected to a TV receiver or monitor with separate Y and C inputs. This does not mean, however, that existing monitors and TV sets with a composite video or SCART input are not suitable for use with an S-VHS recorder. S-VHS equipment is interconnected with special 7-pin terminals and plugs.

A number of semiconductor manufacturers, including Philips Components and Thomson, are currently working on transcoder chips capable of combining Y/C signals into RGB or CVBS. These chips will form the central part in adaptor units installed between the S-VHS VCR and the TV set or monitor. A number of chips are already available for CVBS to-RGB conversion, which, incidentally, should also enable high-resolution colour monitors intended for computer applications (Eizo, NEC, Taxan) to be used for displaying pictures from a TV camera or VCR. The basic application diagram of one of these interface chips, the PAL decoder Type TDA3561 from Philips Components, is shown in Fig. 3.

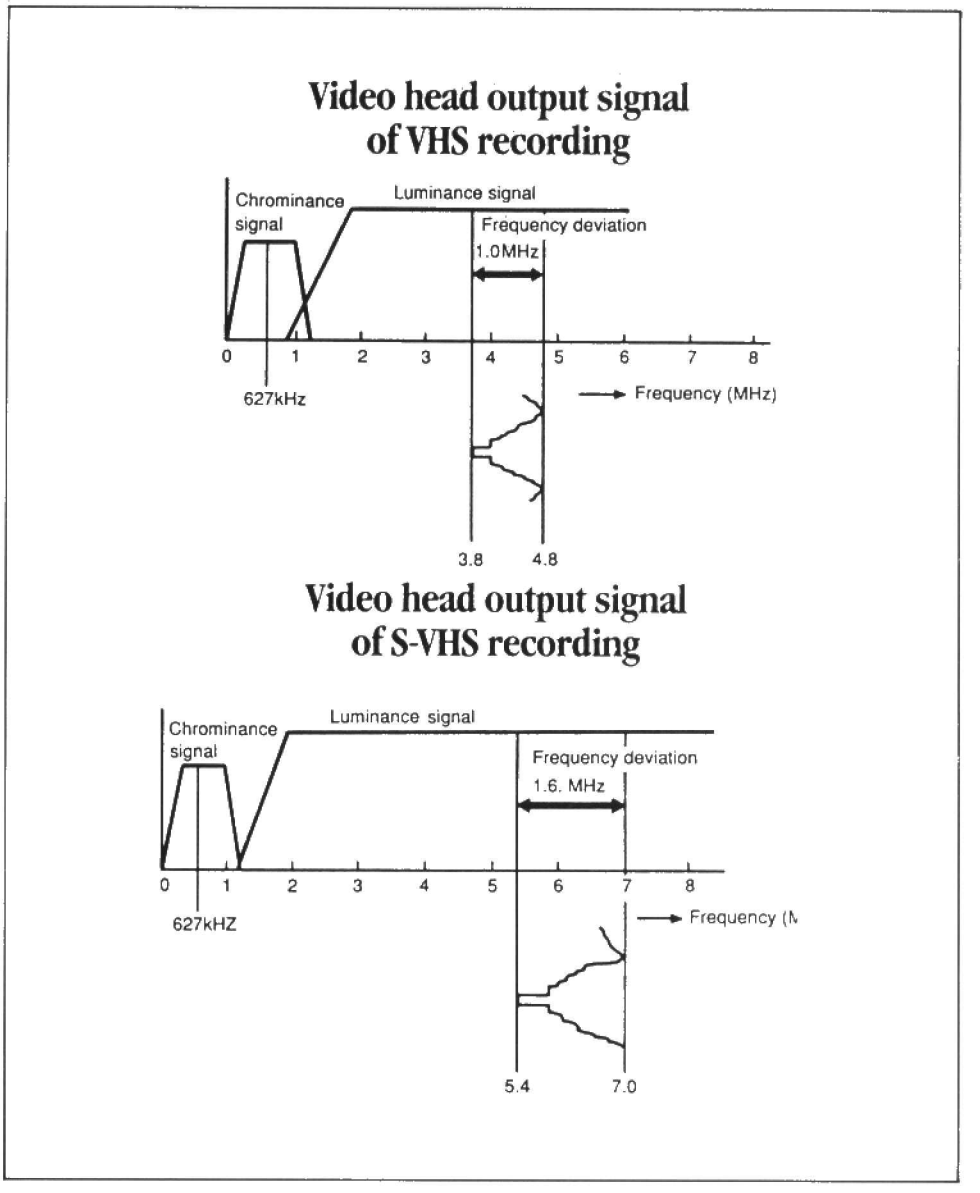


Fig. 1. Spectral comparison of a VHS and a S-VHS signal. The luminance component in the video output signal of the S-VHS recording has been shifted to a higher frequency, and is 1.6 MHz wide, rather than 1.0 MHz.

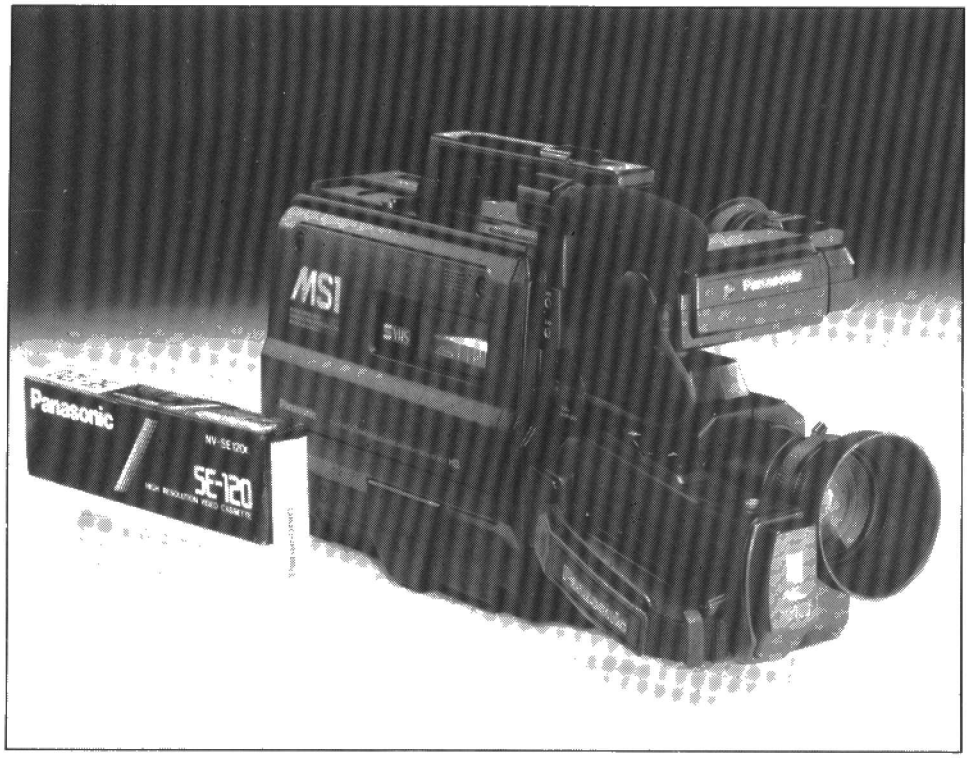


Fig. 2. Panasonic S-VHS camcorder (camera-recorder).

Satellite television

The Astra satellite was successfully launched from Kourou, French Guyana at 0.33 h. GMT on December 11th of last year. At the time of writing this article (mid January 1989), Astra is reported to be on geostationary orbit at 19.2 degrees East, and has successfully completed a number of stages in the testing procedure. The so-called *bus-tests* carried out by engineers at G.E. Astro's headquarters in New Jersey, U.S.A., included testing the satellite's TTC (telemetry, tracking & control) and power subsystems. Initial communications payload tests carried out since 8 January have been successful, as were calibration procedures run by the Betzdorf uplink station in co-operation with British Telecom's International London Teleport. Video and uplink tests are to be run from 25 January, and the satellite is expected to be ready for operational service on 5 February. Initially, the transmitted channels will be Sky Channel, Sky Television News, Sky Movies, EuroSport, ScreenSport, Lifestyle, The Disney Channel, The Arts Channel, The Landscape Channel, the European Business Channel, French and German versions of ScreenSport, Scan-Sat TV3 and ATN-Filmnet.

Meanwhile, Amstrad has launched a low-cost receiving system for Astra, the Amstrad Fidelity (PAL) SRX1000 — see Figs. 4 and 5. The basic system comprises a 60 cm dish, LNB, downlink cable and a 16-channel indoor unit. A decoder for future D-MAC and D2-MAC channels is not yet available because Philips Components have not yet completed the final tests of the Teletext chip in their multi-standard MAC decoder, which is installed as a set-top box.

The Confederation of Aerial Industries (CAI), in co-operation with Astra and the City and Guilds of London, are endorsing special 'hands-on' courses for TVRO installers at a number of technical colleges in the UK.

Digital Picture Processing: an introduction

The advent of RISC (reduced instruction set computer) systems is clearly leading to run-time picture processing with the aid of software algorithms. Radiologists and other medical scientists use powerful computer and scanning systems to build three-dimensional images of human organs and tissue. These techniques have significant advantages over conventional (2-dimensional) X-ray methods because they enable far greater accuracy to be achieved. The advantages are obvous: 3-D images with a resolution of 2 mm give surgeons a good initial impresion of the 'work area'.

Picture processing (DPP) is also essential in astronomy. For instance, the pictures sent by the Giotto spacecraft of the nucleus of the Halley comet could not have been interpreted without virtual real-time processing in large computer systems.

Digital picture processing is basically a way of eliminating noise and improving contrast in a picture by means of error-correcting algorithms. Certain parts of

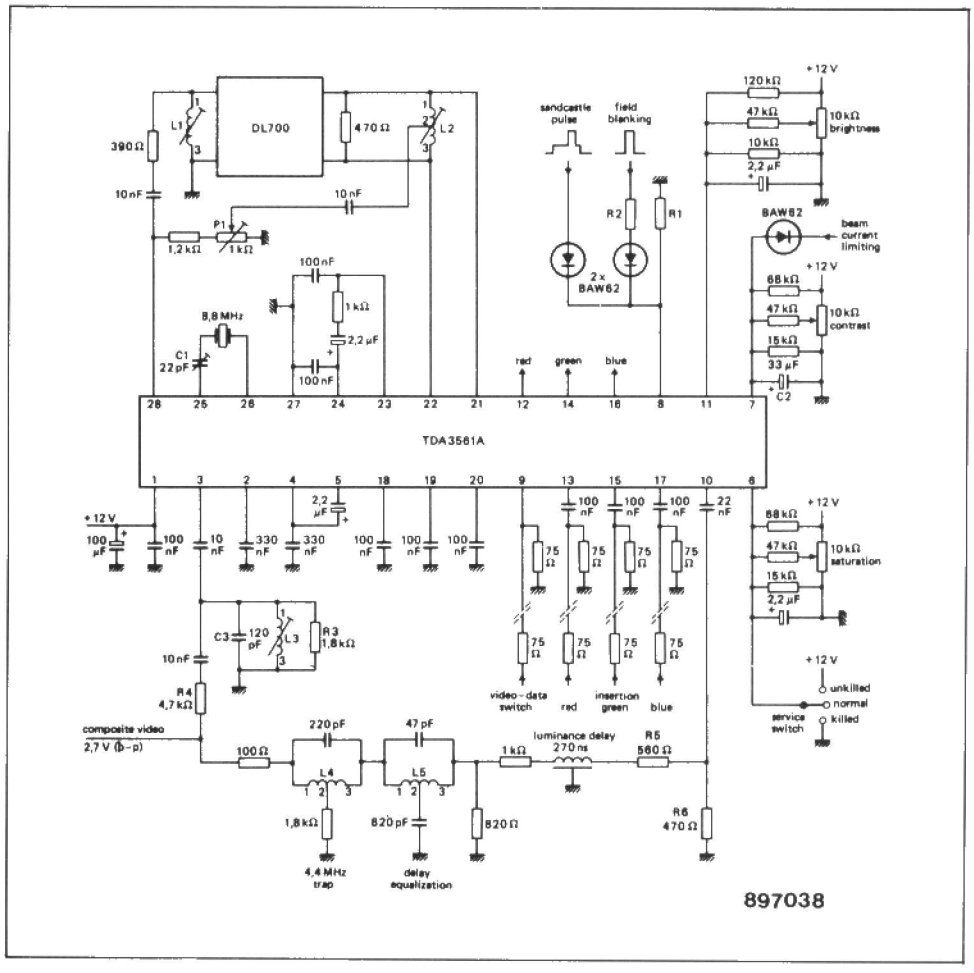


Fig. 3. Application circuit of the TDA3561A PAL decoder (courtesy Philips Components).

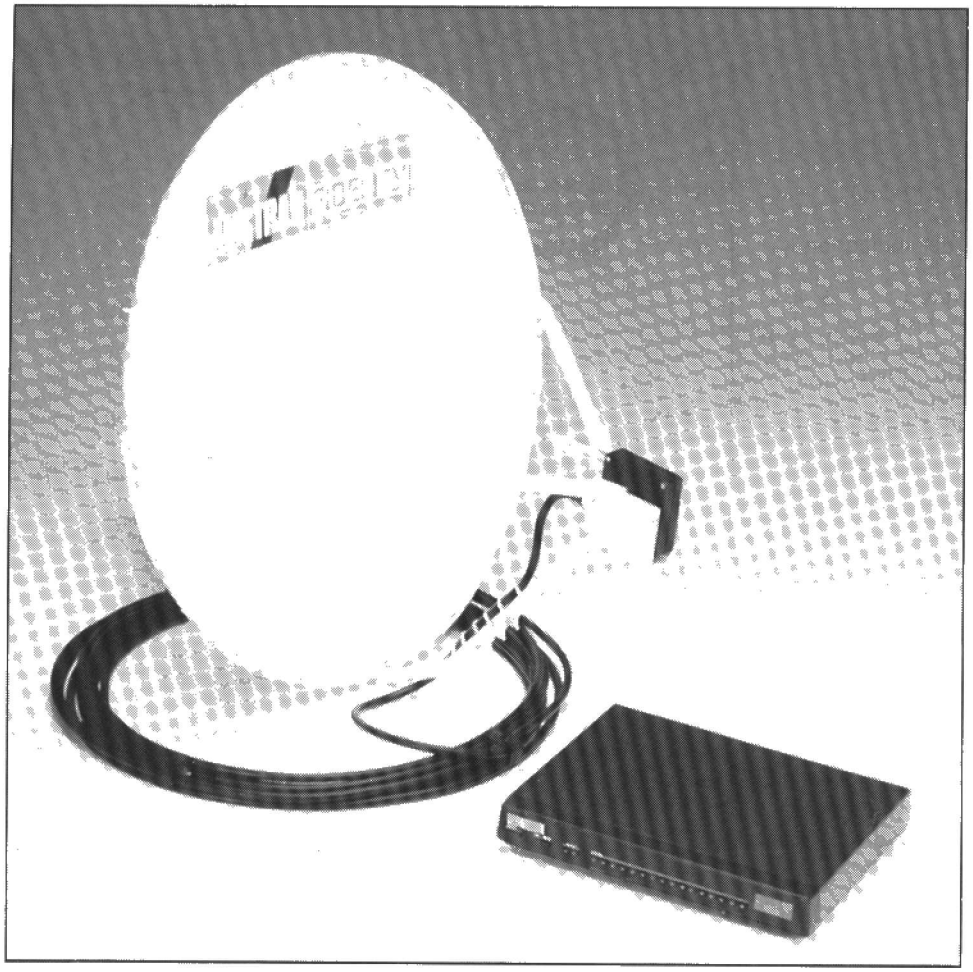


Fig. 4. Amstrad SRX1000 satellite TV reception system.

Fig. 5. Thanks to its relatively high transmit power, the Astra TV satellite can be received with a 60 cm dish, which may be mounted unobtrusively.

the picture can be given extra contrast; information can be added, substituted or deleted. Some algorithms also allow 'subtracting' one picture from another to detect the differences (motion compensation). Similarly, modern meteorology uses picture addition to obtain photographs that show both land contours and weather information such as occlusion charts.

Practical picture processing: RISC does it

One interesting application of DPP is the retouching of damaged or incorrectly exposed photographs. Examples of the use of AIM, a Public Domain DPP software package for the RISC-based Acorn Archimedes computer, are given in Figs. 6 and 7. The left-hand photograph of the moon surface (Fig. 6) is almost unintelligible. After running a so-called *equalization routine*, however, the grey shades are enhanced, resulting in a marked contrast improvement — see the right-hand photograph.

Many modern facsimile machines use a combination of software and hardware for cleaning up messages (pictures) that have been corrupted by noise. The two pictures in Fig. 7 demonstrate the capability of AIM in this respect. After two passes of a noise-reduction algorithm applied to the digitized photograph in the top left-hand corner, the original quality is virtually restored.

Hardware-based error correction has been with us for some time — the

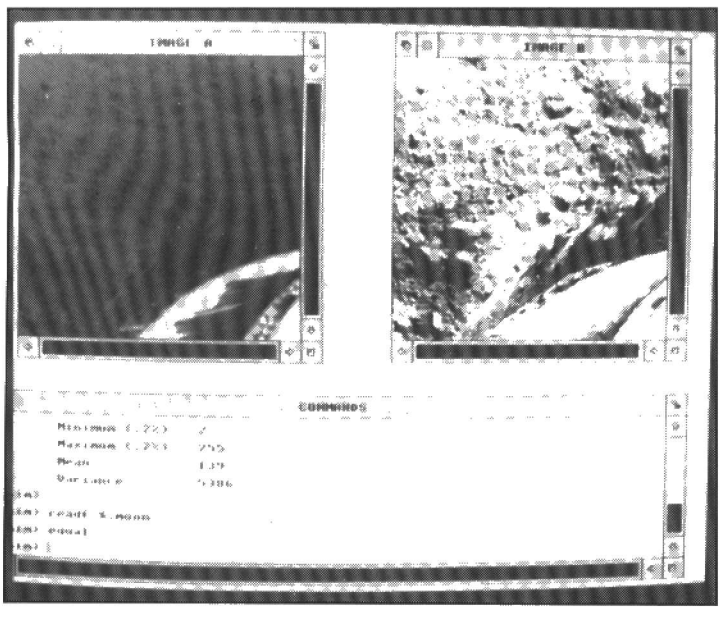


Fig. 6. A photograph of the moon surface made during one of the Apollo flights can be retouched with the aid of AIM, a digital picture processing program for the Acorn Archimedes.

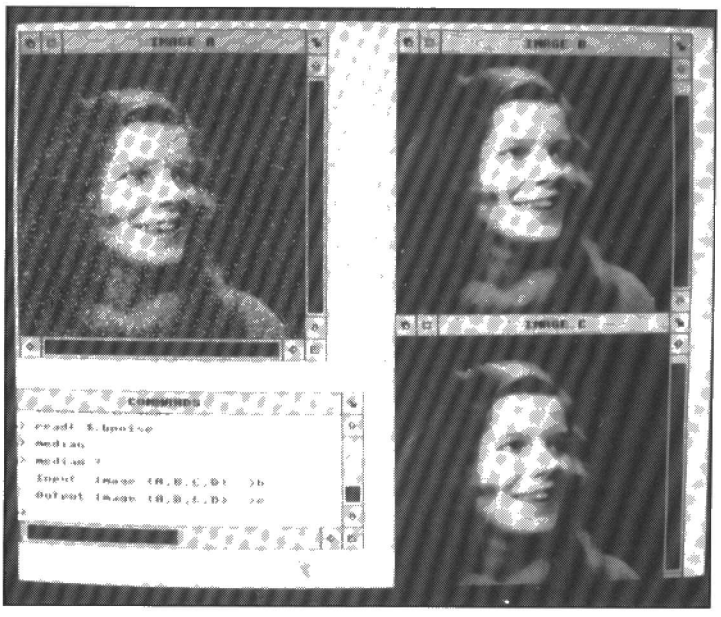
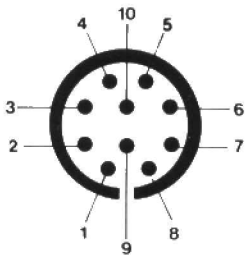


Fig. 7. A two-pass noise suppression algorithm in AIM is capable of suppressing noise in digitized pictures.

K10
The Type K10 video connector is widely used on VHS equipment. The pinning of the K10 connector differs slightly between manufacturers.



87282-1

JVC and related products

pin	signal
1	video in/out
2	ground (video)
3	battery indication
4	power supply in/out
5	audio out
6	start/stop
7	audio in/out
8	ground (audio)
9	ground (power supply)
10	supply (+12 V)

HITACHI

pin	signal
1	video in
2	ground (video)
3	video out
4	record (−9 V)
5	audio out
6	start/stop
7	audio in
8	ground (audio)
9	ground (power supply)
10	supply (+12 V)

PANASONIC (WV series)

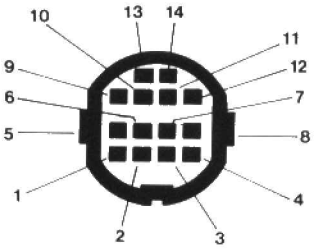
pin	signal
1	video in/out
2	ground (video)
3	not used
4	recorder indication
5	stand by
6	start/stop
7	audio in/out
8	ground (audio)
9	ground (power supply)
10	supply (+12 V)

PHILIPS

pin	signal
1	video in/out
2	ground (video)
3	not used
4	recorder indication
5	not used
6	start/stop
7	audio in/out
8	ground (audio)
9	ground (power supply)
10	supply (+12 V)

PANASONIC (WVP series), CANON, OLYMPUS

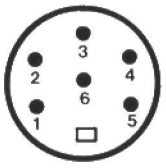
pin	signal
1	video
2	ground (video)
3	serial data
4	serial clock
5	stand-by
6	start/stop
7	audio in/out
8	ground (audio)
9	ground (power supply)
10	supply (+12 V)



87282-2

K14
The pinning of the K14 connector for Betamax equipment is, fortunately, uniform:

pin	signal
1	video out
2	ground (video)
3	video in
4	ground
5	start/stop
6	tally signal
7	microphone-2 out
8	recorder check
9	microphone-1 out
10	ground (microphone)
11	microphone-1 in
12	microphone-2 in
13	supply (+12 V)
14	ground (power supply)

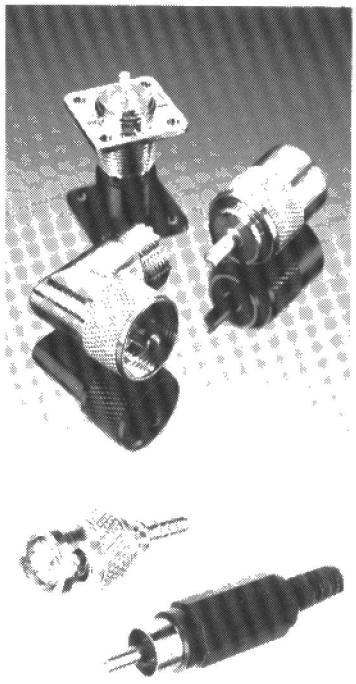


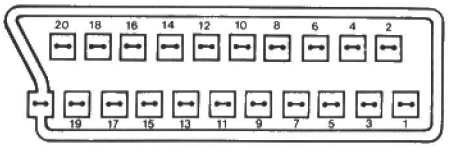
87282-8

DIN connectors
A simple 6-way connector system to DIN45322 is often used in low-cost AV (audio/video) links:

pin	signal
1	control voltage (off = +12 V)
2	video out
3	audio left in/out
4	power supply
5	audio right in/out

HF video connectors (BNC, PL/SO239 and CINCH/RCA)
These plugs, in spite of their different appearances, are all essentially co-axial with the body connected to ground and the central pin carrying the signal. BNC types are available in 50 and 75 Ω versions, PL/SO-239 types only in 50 Ω.





SCART connectors
Virtually all modern video equipment is fitted with a SCART connector. The pin assigment is uniform among manufacturers, but in some cases not all pins are used.

pin	signal
1	audio out R or Ch. 2
2	audio in R or Ch. 2
3	audio out L or Ch. 1 (or mono)
4	ground (audio)
5	ground (blue)
6	audio in L or Ch. 1 (or mono)
7	blue
8	control voltage
9	ground (green)
10	not used
11	green
12	not used
13	ground (red)
14	not used
15	red
16	blanking (active high)
17	ground (video)
18	ground (blanking)
19	CVBS out
20	CVBS in
21	conector shield and/or ground

Overview of video connectors and their pinning

```
 10REM>FILTEMUL/2
 20MODE20
 30 INPUT"Sweep over how many octaves (0 = CW) "oct%
 40 INPUT"Signal-to-noise ratio in dB "K
 50 INPUT"Pink-factor for noise (1=white noise; >1=pink noise) "P%
 60K=1/(10^(K/20))
 70 INPUT"Co-efficient a for Y(T)=a.x(T)+(1-a)Y(T-1) "A
 80IF A<0 OR A>1 THEN 70
 90 INPUT "Order of filter "ord%
100PROCsweep
110PROCnoise
120PROCnoisy_signal
130PROCfilter
140GCOL0,1:MOVE0,800:FORT%=0TO1279STEP3:PLOT5,T%,S(T%)+800:NEXT
150REM -- NOISE ---MOVE0,400:FORT%=0 TO 1279:PLOT5,T%,N(T%)+400:NEXT
160GCOL0,2:MOVE0,500:FORT%=0TO1279:PLOT5,T%,SN(T%)+500:NEXT
170GCOL0,3:MOVE0,200:FORT%=0TO1279:PLOT5,T%,F(T%)+200:NEXT
180END
190:
200DEFPROCsweep
210 REM --- SINE-WAVE DATA ---
220DIM S(1280)
230W=.003*PI
240FORT%=0TO 1280
250S(T%)=100*SIN(W*T%*(1280+oct%*T%)/1280)
260NEXT
270ENDPROC
280:
290DEFPROCnoise
300REM --- NOISE DATA ---
310DIM N(1280)
320FOR T%=0 TO 1280
330N(T%)=K*(RND(100)-RND(100))
331IF P%<2 THEN 390
340noise=N(T%)
350FOR n%=0 TO P%
360N(T%)=noise
361IF T%=1280 ENDPROC
370T%+=1
380NEXT n%
390NEXT T%
400ENDPROC
410:
420DEFPROCnoisy_signal
430DIM SN(1280)
440SN()=S()+N()
450ENDPROC
460:
470DEFPROCfilter
480DIM F(1281)
490FOR T%=1 TO 1279
500F(T%)=A*SN(T%)+(1-A)*F(T%-1)
510NEXT
520 FOR ord%=1 TO ord%
530FOR T%=1 TO 1279
540F(T%)=A*F(T%)+(1-A)*F(T%-1)
550NEXT
560NEXT
570ENDPROC
580:
```

Fig. 8. Acorn Archimedes program that demonstrates some basic procedures in signal recovery from noise.

modern CD player is an example of this. Analogue signals corrupted by noise can also be 'cleaned' by the RISC computer. The listing of Fig. 8 is a demonstration program written in BBC BASIC V. It should be borne in mind that the program is only intended to become acquainted with the basics of software-based filtering of noisy signals. The program as shown may be modified for running on other computers than the Archimedes, but calculation times will be unacceptable in many cases. The program prompts the user to enter the desired signal-to-noise ratio and the order of the filter, and demonstrates the possibility of recovering, in theory, a signal even when this has an S/N ratio of 0.

The hardware approach to noise filtering may be demonstrated with the basic ciruit shown in Fig. 8. The filter is usable for signals between 100 and 2500 Hz, and can be clocked by an external source (5 to 60 kHz).

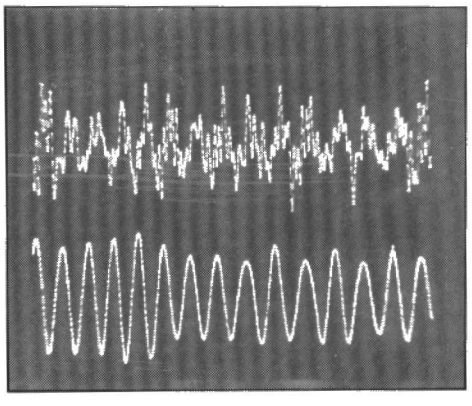


Fig. 10. The results of the circuit of Fig. 9 are remarkable given the simplicity of the design.

There is very little doubt that RISC-based computer systems running dedicated error-correction software will eventually become so fast as to enable run-time, digital, enhancement of video signals. This has been partially achieved already with a combination of hardware and software MAC TV decoders, of which the first types are expected to become available commercially later this year.

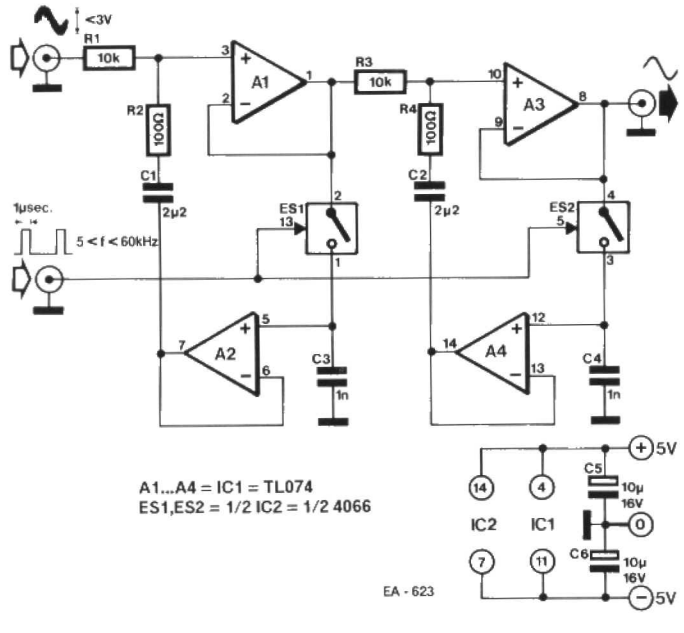


Fig. 9. Experimental noise-suppression circuit.

NEW BOOKS

Correction
In the New Books section of February 1989, the price of the two volumes of "Television Engineering" was erroneously stated as £00.00. The price for each volume should have read £24.00. We apologize for any inconvenience caused.

Solving Problems in Electrical Power and Power Electronics

by H.F.G. Gwyther
ISBN 0 582 28644 1
203 pages — 245 × 185 mm
Price £9.95 net (soft cover)

This new book forms part of the "Solving Problems in..." series. This is a major series intended for engineering students at universities, polytechnics and colleges. Some titles deal with elementary work; others cover advanced topics. Each chapter contains a summary of essential theory, worked examples demonstrating the application of theory in solving examination type questions and further examples (with answers) for practice.

Since real problems in industry often bring together several aspects of Electrical Engineering, it is essential that all students of Electrical Engineering receive a grounding in a broad range of topics before specializing in a particular area in their final year. One subject which must be looked at is the topic of Electrical Power and Power Electronics. "Solving Problems in Electrical Power and Power Electronics" meets the need for a text based on worked examples and examination-type questions. Contents include the transformer, electromechanical energy conversion, fault protection and surges, and electrical power distribution systems.

The book is recommended to all students of Electrical and Electronic Engineering at degree and higher technician level, and also to teachers and lecturers as a handy source of questions for tutorials.

Longman Scientific & Technical • Longman House • Burnt Mill • HARLOW CM20 2JE.

An Introduction to Loudspeakers and Enclosure Design

by V. Capel
ISBN 0 85934 201 8
148 pages — 178 × 110 mm
Price £2.95 (paperback)

How does one optimize the sound properties of a loudspeaker enclosure? Where should the enclosures be placed to ensure that the sound reproduction is acoustically best? These, and other questions, are answered in Vivian Capel's latest book.

Apart from loudspeakers and boxes, the book also deals with crossover filters and the question "What parameters matter?".

The book finishes with a step-by-step description of the construction of the Kapellmeister loudspeaker enclosure originally published in *Electronics Today International*.

Vivian Capel is well-known for his articles that have appeared in the technical press for over thirty years. He is the author of a dozen books on audio, acoustics and related subjects.

More Advanced Electronic Security Projects

by R.A. Penfold
ISBN 0 85934 164 X
95 pages — 178 × 110 mm
Price £2.95 (paperback)

Intended primarily as a sequel to the earlier published "Electronic Security Devices", this book provides a number of slightly more complex projects that should be within the capabilities of most electronics hobbyists, and even beginners. Ease of construction is ensured by the provision of stripboard layouts in all cases.

Although the projects are not substantially more complex than those in the earlier book, they do use more advanced techniques. The projects include a passive infra-red detector that can be used with a variety of lens systems, a fibre-optic loop alarm, computer-based alarms and an unusual form of ultrasonic intruder detector.

LOGO for Beginners

by J.W. Penfold
ISBN 0 85934 167 4
88 pages — 178 × 110 mm
Price £2.95 (paperback)

This book is an introduction to the programming language LOGO and to computing, as it assumes no previous knowledge of computers or programming.

LOGO is a good language to learn programming, indeed, that was its original purpose. It teaches how to write programs in a structured form which makes them easy to follow and to understand. The book starts with the famous turtle graphics and then goes on to explore the mathematical and logical aspects of LOGO, and finally to the interesting topic of list processing, on which many aspects of artifical intelligence are based.

Bernard Babani (Publishing Ltd • The Grampians • Shepherds Bush Road • LONDON W6 7NF.

Electronic Fault Diagnosis

by G.C. Loveday
ISBN 0 582 02358 0
132 pages — 245 × 188 mm
Price £6.95 (soft cover)

The ability to rapidly diagnose the cause of faults in electronic equipment and circuits is one of the important skills that can be acquired by the electronic technician or mechanic. This book is intended to serve as an introduction to the subject.

Naturally, fault diagnosis skill is not achieved easily, since it combines a good understanding of component and circuit operation together with knowledge on testing methods and on how components fail.

The exercises throughout the book are designed to assist the student in improving his fault diagnosis technique. The text concentrates mainly on component faults occurring in particular types of circuit rather than on the fault-finding techniques used for localizing faults in complete electronic instruments or systems. There is, however, a section that deals briefly with system fault-finding methods.

The majority of the circuits have been built and tested before measurements are made under fault conditions. It is intended that students should construct or breadboard the circuit as practical project work. For this reason, readily available components have been chosen wherever possible.

This, the third, edition of the book also reflects other important trends in electronics and includes notes and exercises on opto-isolators, timer ICs, SMPU designs and power FETs.

The book is intended primarily for students studying City and Guilds 224 Electronics Servicing and the BTEC Certificate and Diploma courses. It will undoubtedly attract a much wider readership.

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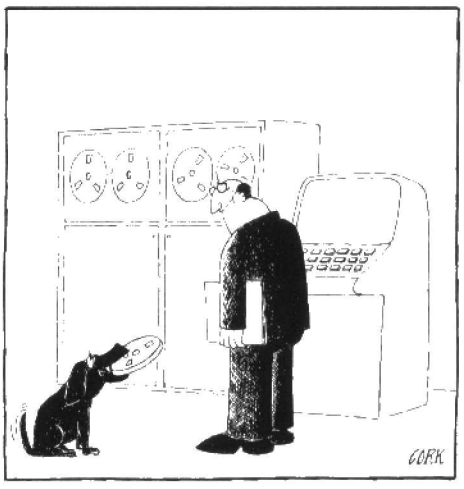


ATN-FILMNET DECODER

by P.N.P. Wintergreen

Anyone in Western Europe in possession of a private reception system for TV satellites must, at some time, have noticed that some channels can not be watched unless an appropriate decoder is bought or rented. Hence, working on descrambler circuits is a popular and highly interesting pastime with technically inclined owners of satellite TV receiving equipment.
In line with this month's feature article on video, this article discusses an ATN-Filmnet decoder that is remarkable for its reliability, selectivity, automatic switch-over capability and low cost. Thanks to its versatile design, the decoder is suitable for use with many commercially available indoor units.

ATN-Filmnet is a satellite pay-TV channel owned by Esselte, a Dutch/Belgian consortium. The channel, which is transmitted via ECS-4 transponder number 9-W-V at 11.138 GHz, is intended mainly for feeding into large cable-TV networks in Holland, Belgium, Scandinavia and, since late last year, France also. In view of the large area serviced by the ECS-4 satellite (formerly ECS-1), English is used as the main language on ATN-Filmnet. Subtitling with synchronous translations in six, viewer-selectable, languages is available as a teletext service. Recently, it was announced that ATN-Filmnet is to transmit via Astra also. At the time of writing this article (early January 1989), it is not known as yet whether the present decoder is suitable for Filmnet's transmissions via Astra.

ATN-Filmnet decoder

- PLL-based synchronization regenerator
- Automatic encoded/non-encoded switch-over
- Digital timing used throughout design
- Video processor is transparent to other satellite TV channels
- Decoder retains multi-language Teletext Service
- Three buffered video outputs: VCR; monitor; remodulator
- Separate FM synchronization receiver module for fitting in indoor unit
- Simple-to-connect to most types of indoor unit, including *Elektor Electronics* IDU
- Few alignment points
- No expensive components
- CMOS design ensures low current consumption

Principles of the coding system

The scrambling system used by ATN-Filmnet is based on SATPAK equipment supplied by Matsushita of Japan. SATPAK is basically an analogue, multimode, video scrambling system with provision for so-called *over-air entitlement control* of individual viewers, who are, therefore, the *subscribers* to the channel. The system is, in principle, designed for distribution of the scrambled programme via a cable network for radio and TV, *not* for private reception direct from a satellite (this was deemed impossible at the time the ECS-1 was taken into service).
Until about two years ago, ATN-Filmnet transmitted unscrambled via satellite; scrambling was effected in the cable head-end stations. The change to scrambling-on-satellite was prompted by the increasing number of subscribers and a growing interest for the programmes in the Scandinavian countries on the one hand, and the availability of equipment for private satellite reception on the other.
In the above mentioned countries, ATN-Filmnet, through a network of local representatives, rents decoders to subscribers, who pay an entrance fee, and in addition a fixed sum for certain time-slots during which action movies are transmitted. Since every subscriber is identified, and allowed to view certain programmes with the aid of a unique digital code recognized in the rented decoder, this unit becomes useless when the subscriber fails to pay his subscription fee. Clusters of subscriber identification and entitlement codes are transmitted continuously with the scrambled programmes, to update the relevant information stored in the decoders during a previous access. Rented ATN decoders are sealed, and it is practically impossible to tamper with the microprocessor-driven decoder circuit inside.

The basic configuration of the building blocks in the scrambling equipment is shown in the schematic drawing of Fig. 1. The 14 GHz uplink transmitter for the 9-W-V transponder on board the ECS-4 satellite is frequency-modulated with a baseband signal that has a band with of 0 to about 8.5 MHz. The first part of this spectrum, 0 to about 5 MHz, is allotted to the composite, scrambled, video signal and the associated PAL chrominance subcarrier. The remainder of the spectrum is assigned to a number of FM subcarriers:

- main sound channel at 6.6 MHz (wide-band FM; uncoded);
- subscription, entitlement and scrambling-mode data at 7.2 MHz (FM)
- composite-sync pulses at 7.56 MHz (FM);
- a stereo radio programme, Radio-Ten at 7.92/8.10 MHz (NBFM; Panda-Wegener compressed).

The video signal is left unscrambled for about half an hour, three times every 24 hours, before the next 'film block' starts. One of these intervals is between 13.45 h and 14.15 h UK time, just between two movies, allowing non-paying viewers to see the week's programme schedule, so as to encourage them to take out a subscription. The present decoder switches on and off automatically, so that a viewable signal is always ensured at its output(s), which are, therefore, perfect for driving a timer-controlled VCR. Correctly aligned, and connected to an indoor unit with good demodulator characteristics, the decoder has a lock-in time of less than one second, is transparent to other satellite TV signals, and works reliably even with fairly noisy signals.

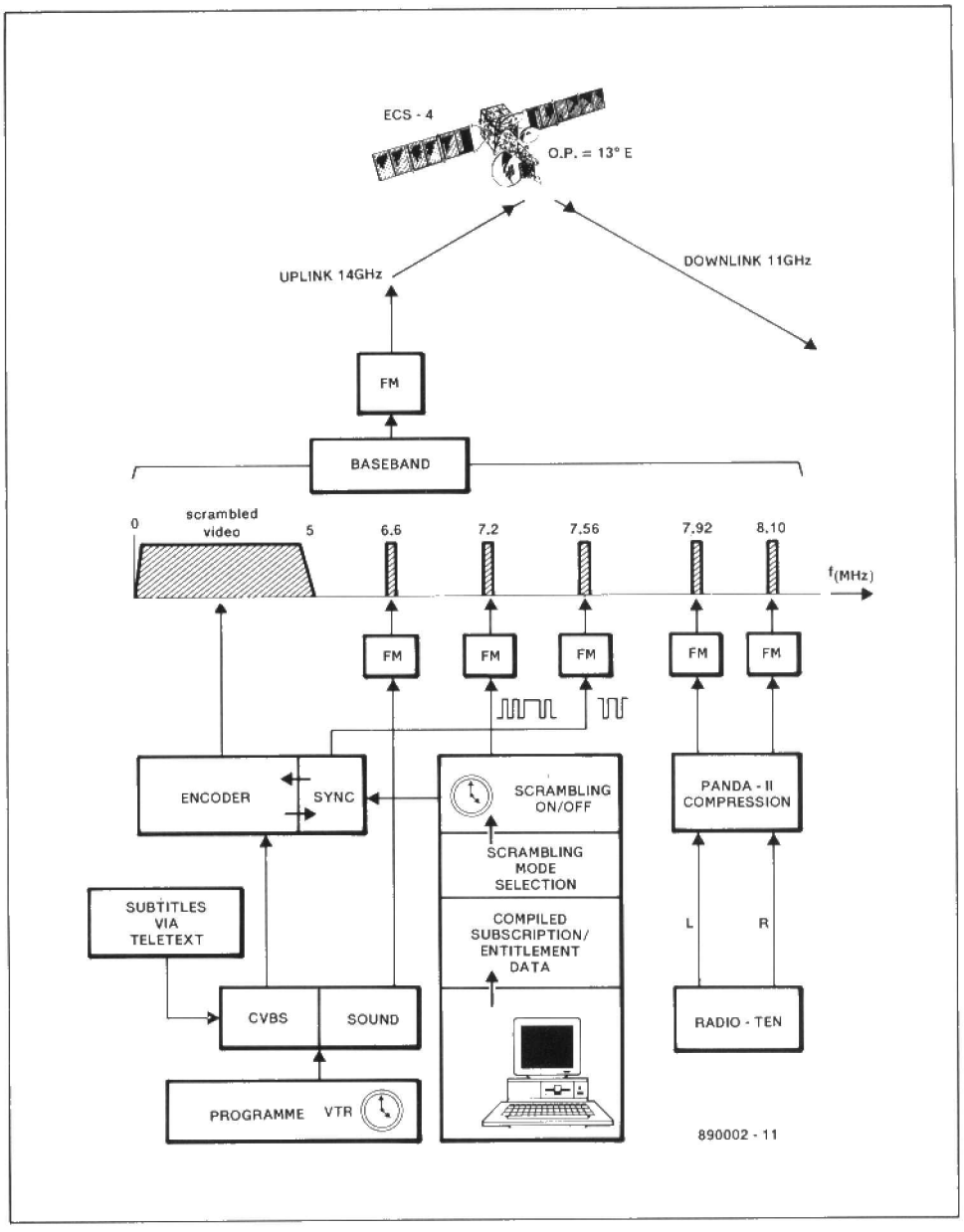


Fig. 1. Schematic representation of the equipment used at the ATN-Filmnet uplink station.

At the receiver side: TVRO and cable systems

In a privately owned receiver system (TVRO; *television receive only*) lined up for reception of ATN-Filmnet on ECS-4, the baseband signal is available as shown in Fig. 2. As will be seen later on, the proposed decoder combines the received composite-sync (*c-sync*) pulses with unclamped video to give a viewable picture. In a practical indoor unit, the section marked CLAMPING shown in the block diagram of the receiver is usually a single circuit that combines the functions of video level clamping and dispersal suppression.

The basic structure of a cable-TV head-end station equipped for carrying satellite TV channels is shown in Fig. 3. Separate receive systems are mounted for each satellite TV channel fed into the cable network. In the case of the remodulator for ATN-Filmnet, the sync

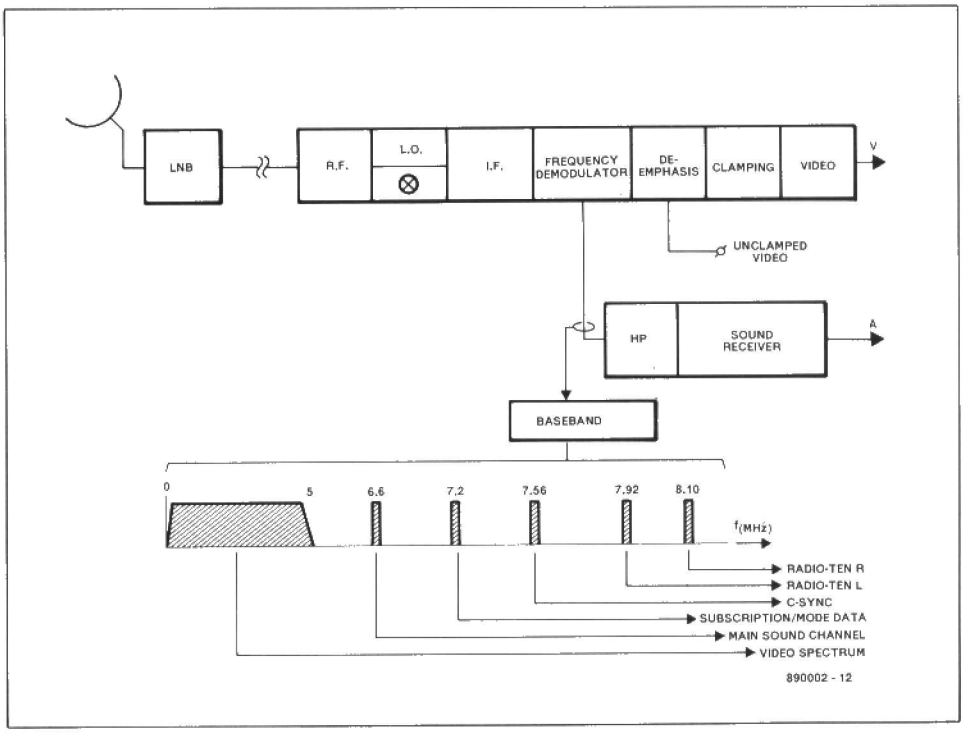


Fig. 2. The complete baseband transmitted by ATN-Filmnet is recovered in a TVRO system.

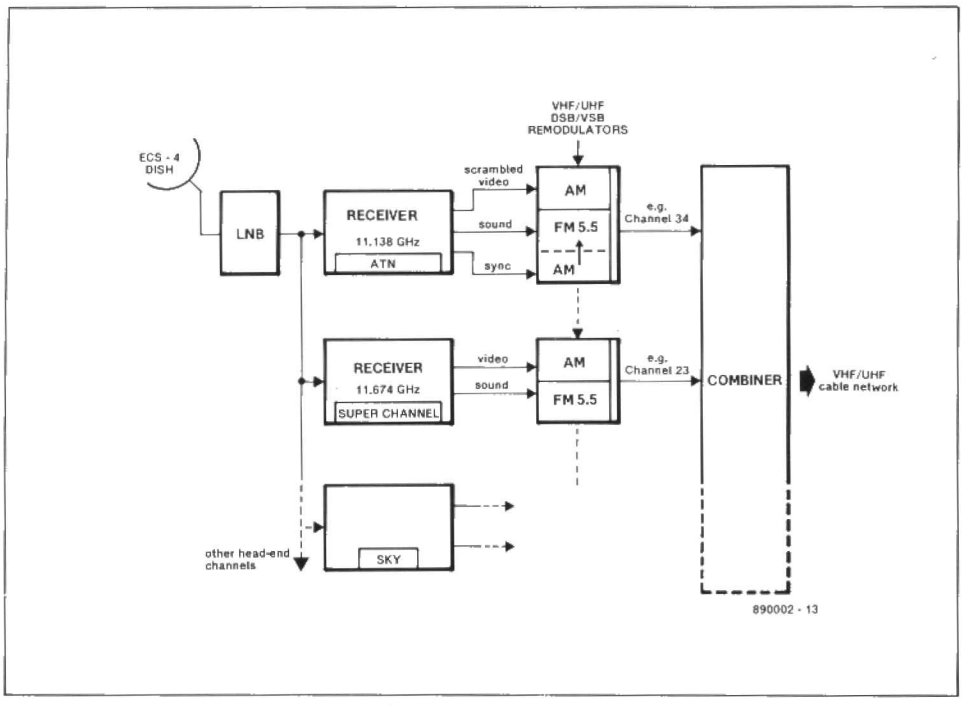


Fig. 3. Partial structure of a cable-TV head-end station equipped for reception of ATN-Filmnet, and feeding the scrambled programmes to subscribers. Note the use of an 'AM on to FM' modulation system for the sync pulses.

pulses obtained from a baseband filter and associated demodulator are *amplitude-modulated* at a low level onto the *frequency-modulated* main sound subcarrier at 5.5 MHz above the vision carrier. By virtue of the high AM-suppression of the FM sound demodulator in modern TV sets, the sync pulses are normally inaudible. Rented decoders have a built-in VHF/UHF tuner which is set to the relevant cable-channel assigned to ATN-Filmnet. A special 5.5 MHz-offset, AM, detector is fitted to supply the c-sync signal. The process of descrambling, mode switching and block timing is internal to the rented decoder, and, therefore, completely invisible to the paying subscriber.

Pulse receiver and principle of decoding

Since the proposed circuit is intended as an add-on unit for indoor units, the subject of cable-TV will no longer be referred to.

The most essential signal for the decoder is the composite-sync signal, which is extracted from the baseband with the aid of a simple FM pulse-receiver tuned to 7.56 MHz. This circuit is a standard application of the well-known Type TBA120S quadrature demodulator (see Fig. 4). Input filter L_1 and quadrature coil L_2 are both tuned to 7.56 MHz. The de-emphasis capacitor, C_4, has a relatively low value here to ensure sufficient suppression of the 15.12 MHz quadrature product, and to keep distortion of the demodulatred line-sync component at 15,625 Hz as low as possible (distortion leads to phase-rotation). The composite sync signal is supplied to the decoder by buffer T_1.

Owing to the limited bandwidth of the 7.56 MHz sync channel, the pulses are distorted to Gaussian shapes as shown in timing diagram Fig. 5c. Since, in spite of good picture quality, the sync signal will typically have a signal-to-noise ratio of only 10 to 20 dB, a relatively broad noise-band will be observed when an oscilloscope is used to display the demodulated c-sync signal (this noise is not shown in the timing diagram of Fig. 5c).

It will be clear that the 'noisy' sync pulses received at 7.56 MHz need filtering without affecting the phase relation to the scrambled video signal in the baseband. It is for this reason that the c-sync signal is *regenerated* in the actual decoder with the aid of a phase-locked loop (PLL), whose operation will be detailed below.

Coding and decoding: the principles

So how is ATN Filmnet actually coded, and what is the function of the c-sync signal in all this? The answers are given by timing diagrams a and b in Fig. 5. The video signal is scrambled by inverting its polarity during each even-numbered raster in the frame (a *frame* is composed of two interlaced *rasters*, or *fields*). The first task of the decoder is, therefore, to determine, automatically, the polarity of a raster to decide whether or not this has to be inverted. That is not the whole story, however, since, in spite of correct polarity, the video signal will still fail to synchronize on the TV. Again referring to Figs. 5a and 5b, this is due to the level of the sync pulses relative to the video information. Fig. 5b shows the simplified waveform of the scrambled signal. The lowest level, 0%, is formed by the bottom of the sync pulse, but also by the black level of the video signal,

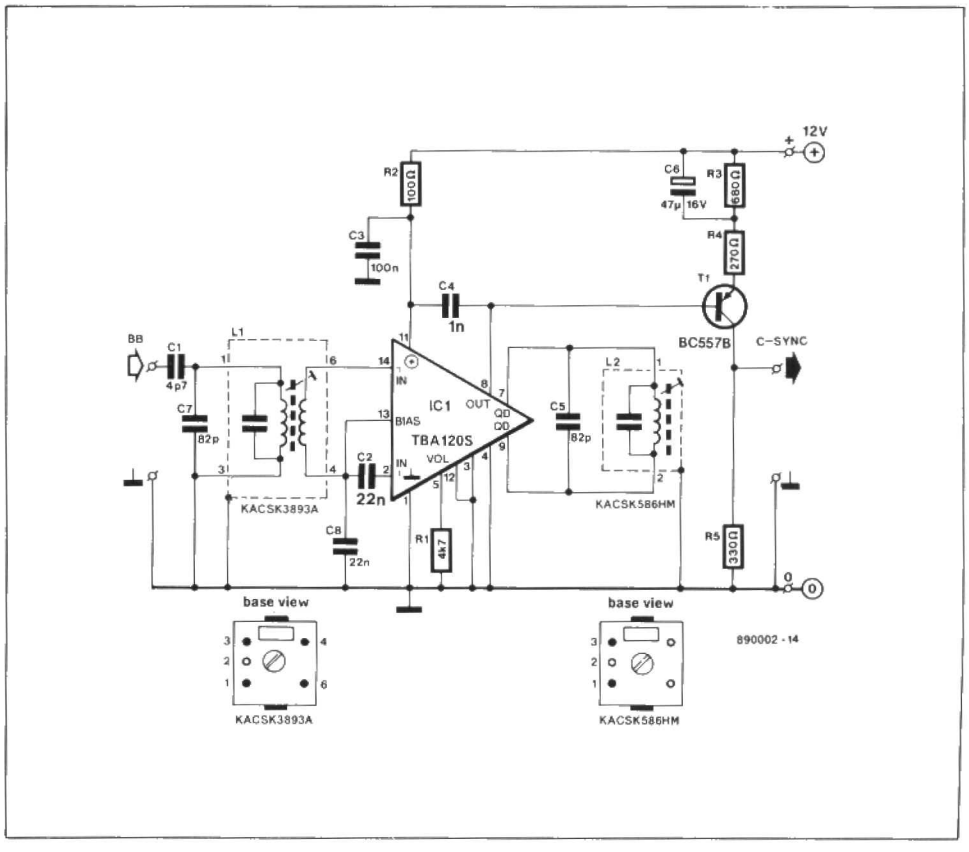


Fig. 4. Circuit diagram of the 7.56 MHz pulse-receiver. The inductors used are ready-made types from Toko.

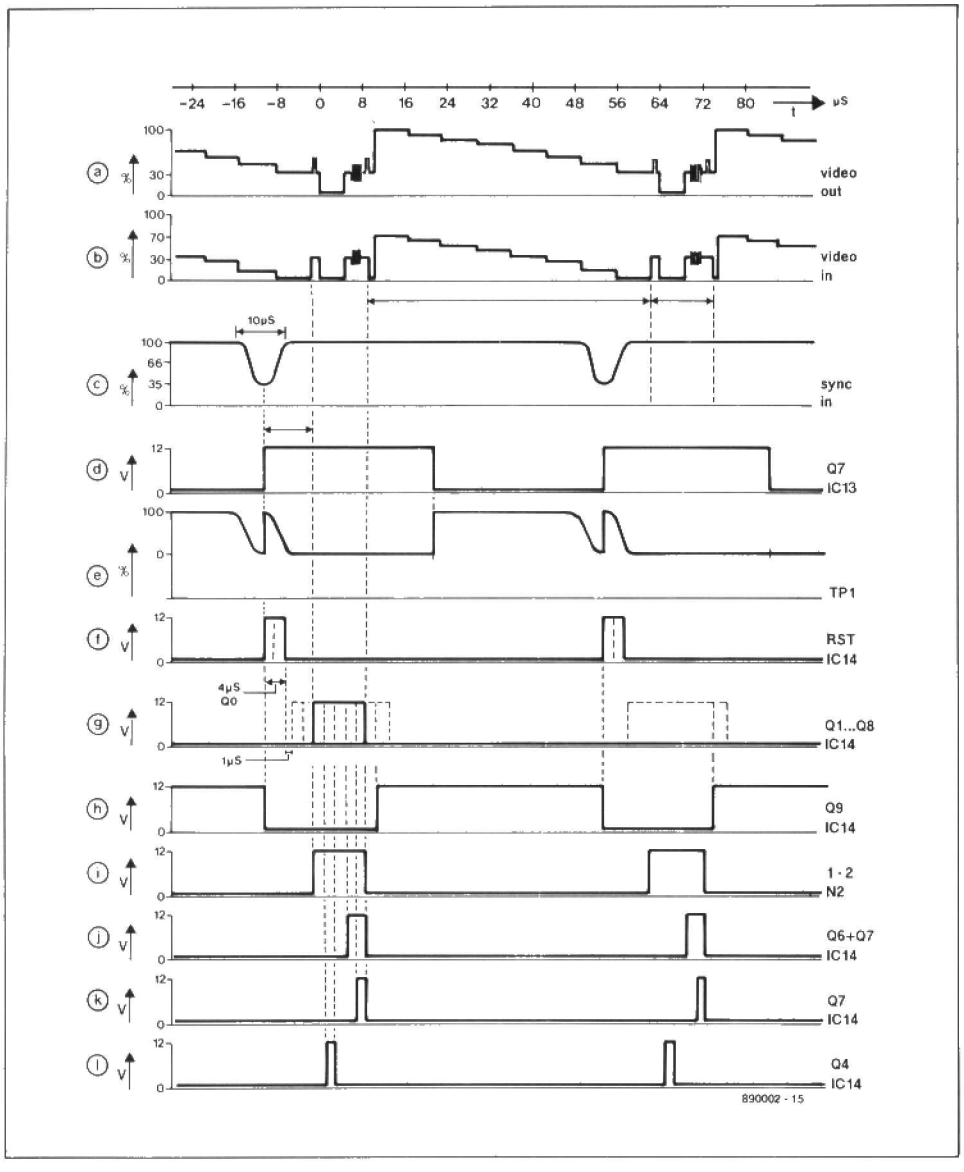


Fig. 5. Timing diagrams that explain the operation of the decoder circuit.

which is normally at about 30% (see Fig. 5a). This scrambling method causes the sync separator in the TV set to mistake a certain instantaneous black level in the video information for sync pulses, so that picture synchronization is not, or hardly ever, achieved.

Since the previously mentioned PLL is by definition capable of providing frequency and phase information on the line sync, it becomes possible to shift 52 µs of the video content of every line upwards by 30%.

The structure of the scrambled video on ATN Filmnet is fairly simple once it is agreed that the level ratio of sync-to-blanking is correct, but the absolute level of the video 30% too low, instead of the other way around (sync 30% too high). As apparent from Fig. 5a, the blanking level, which is normally at 30%, has a constant level somewhere in the middle of the video range. The blanking level of the decoded signal is kept stable by a control signal obtained from a comparison of the blanking level of the scrambled signal with its inverted counterpart. This approach results in flawless switching between the two signals in lines 5 and 318 of the TV picture.

The instant that the circuit switches over to the other polarity of the unclamped video signal is determined by the sync signal supplied by the 7.56 MHz FM receiver, a delay circuit, and a counter for half-lines. This instant is indicated by the vertical dashed line in Fig. 6. The negative-going pulses in the composite sync signal, shown in diagrams Fig. 6a and 6c, represent the line-sync pulses, the 'block' is the field sync. After detection of the field sync pulse, a delay of 112 µs is introduced before the half-lines counter is reset to mark the start of its counting operation. Polarization inverting is effected after 8 half-lines. When the counter has reached state 633, polarization is again inverted, and the counter advances to 1250 half-lines before it is reset during line 1.

Circuit description: not for the faint-hearted

The practical circuit of the ATN Filmnet decoder, shown in Fig. 7, is an interesting example of the combined use of digital and analogue electronics. The design is based throughout on commonly available, inexpensive, parts.

Phase-locked loop and scrambling detector

The composite-sync signal supplied by the 7.56 MHz receiver (Fig. 4) has an amplitude of about 1 V_{pp}, and is applied to a difference amplifier set up around T_{18} and T_{19}. In this amplifier, T_{17} functions as a 2 mA constant-current source. Preset P_3 allows setting the balance between the two output signals developed across R_{64} and R_{65}. The complementary output signals are applied to a phase comparator composed of electronic switches ES_9 and ES_{10}. The switches are closed alternately by a 15,625 Hz, rectangular, signal supplied by output Q7 of counter IC_{13}. This IC divides the 4 MHz signal supplied by voltage-controlled oscillator (VCO) T_{20}-T_{21} by 256 (see also Fig. 5d). A low-pass loop-filter built around opamp A_4 supplies the VCO control voltage, and closes the phase-locked loop.

The 4 MHz VCO around T_{20} is a Colpitts type. The frequency of oscillation is determined by the voltage across varicap D_{23}, which forms part of an L-C tuned circuit. Transistor T_{21} raises the oscillator signal to a digital level, while N_9 functions as a buffer.

If the VCO has been set to 4 MHz, the PLL will lock when a sync signal is present at the relevant input. In that condition, and with P_3 correctly aligned, test point TP1 carries a signal as shown in Fig. 5e. The average amplitude of this signal is 50%, as is always the case for a locked PLL circuit.

In a second phase comparator, ES_7-ES_8, the phase difference is smaller than 90°. As a result, the phase comparator generates an error signal, which is basically a direct voltage. After filtering in C_{19} and C_{21}, this voltage causes comparator A_3 to toggle. LED D_6 then lights, and the decoder is switched from stand-by to the actuated state. Inverter N_3 interrupts the current flow through D_2, so that the emitter voltage of T_{15} rises, and the field-sync separator around T_{15} and T_{16} is enabled.

Timing

At the start of each raster, the field-sync separator supplies a pulse to inverter N_4, which, in turn, supplies a digital clock pulse to bistable FF_1. Differentiating network C_{22}-R_{55}, and diode D_4, cause FF_1 to reset counter IC_9 only once during every frame. The time difference between the block pulse and the reset pulse is determined by R-C network P_2-C_{20}. The required delay of 112 µs is adjusted with the preset.

After the reset pulse, IC_9 starts to count

from 0 at the double line rate. Eight clock cycles later, counter output Q3 goes high and clocks FF_2. This causes ES_1 to open, so that the non-inverted video is fed to the decoder output.
After 625 half-lines, the cathodes of D15 through D19 are all logic high simultaneously, so that bistable FF_4 is clocked. This generates a polarization test-pulse, which is active low and has a length of 4 lines. The end of this pulse is marked by the video-inversion toggle instant, which occurs after 633 half-lines. Bistable FF_3 is then clocked so that FF_2 is reset. This results in ES_1 closing, and ES2 opening.
The video signal now has the correct polarity at all times, but must be brought to a 30% higher level, without, of course, affecting the sync and blanking levels. As evident from Figs. 5c and 5d, the lowest amplitude of the received line-sync pulse at 7.56 MHz coincides with state xxxx00000000 of IC_{13}. A diode-based OR gate at the output of this counter supplies a 4 μs-long reset pulse to a further counter, IC_{14} (see Fig. 5f). Next, N_6 adds 1 μs to the delay, so that IC_{14} receives its first clock pulse after 5 μs (the delay is either 4 or 5 μs as set with a jumper). As shown in Fig. 5g, the outputs of IC_{14} go logic high at 2 μs-intervals. When, finally, Q9 goes high, the counter blocks its own clock pulses. The counting process is stopped, and is not restarted until a new reset pulse is applied. Counter outputs Q3 through Q8 are connected to a diode-AND network, D_{30}-D_{34}, and so supply a pulse that coincides with the blanking and line-sync (see Fig. 5i). This pulse times the shifting by 30% of the synchronization pulses relative to the video information. Outputs Q6 and Q7 of IC_{14} are always high during the blanking period in the video signal. This time-slot (Fig. 5j) is derived with the aid of diodes D_{28} and D_{29}, which control a sample-and-hold circuit that samples the blanking levels of the true and inverted video signals. Counter output Q4 is high during the line-sync (see Fig. 5l).

Automatic polarity correction

Comparing the instantaneous amplitude of the output video signal during the line-sync interval with that during the line-blanking interval produces a difference signal whose sign enables the polarity of the video signal to be deduced (see Fig. 5k). The circuit to do so is set up around T_{12}, T_{13} and T_{14}. Electronic switches ES_5 and ES_6 sample the scrambled video signal. If this has the right polarity, the voltage on C_{11} will be lower than that on C_{12}, because C_{11} is charged during the sync periods, and C_{12} during the blanking periods. When the time for a half-picture (*raster*) has lapsed, bistables FF_3 and FF_4 generate the polarization-test pulse. This pulse supplies T_{12} and T_{13} with a tail current via R_{41}. Only T_{13} conducts, however, because its base is at a higher potential than that of T_{12}. Nothing happens until the raster is inverted, since this results in U_{C11} becoming higher than U_{C12}, so that T_{12} conducts during the test-pulse. T_{14} then conducts also, and resets IC_9. This action takes place exactly one raster earlier than under normal circumstances, ensuring the required polarity by shifting the phase of the picture contents by 180°.

Video processing

The unclamped video signal supplied by the indoor unit is fed to a difference amplifier around T_1 and T_3, with T_2 functioning as a current source. Because of the constant current in the collector lines of T_1 and T_3, the sum of the voltages developed across R_3 and R_5 is constant:

$$I_{R3}+I_{R5} = \text{constant}$$
$$I_{R3}+R_4+I_{R5}+R_5 = \text{constant} \quad (R_3=R_5)$$
$$U_{R3}+U_{R5} = \text{constant}$$

The amplified video signal is available in true and inverted form across R_5 and R_3 respectively. Electronic switches ES_3 and

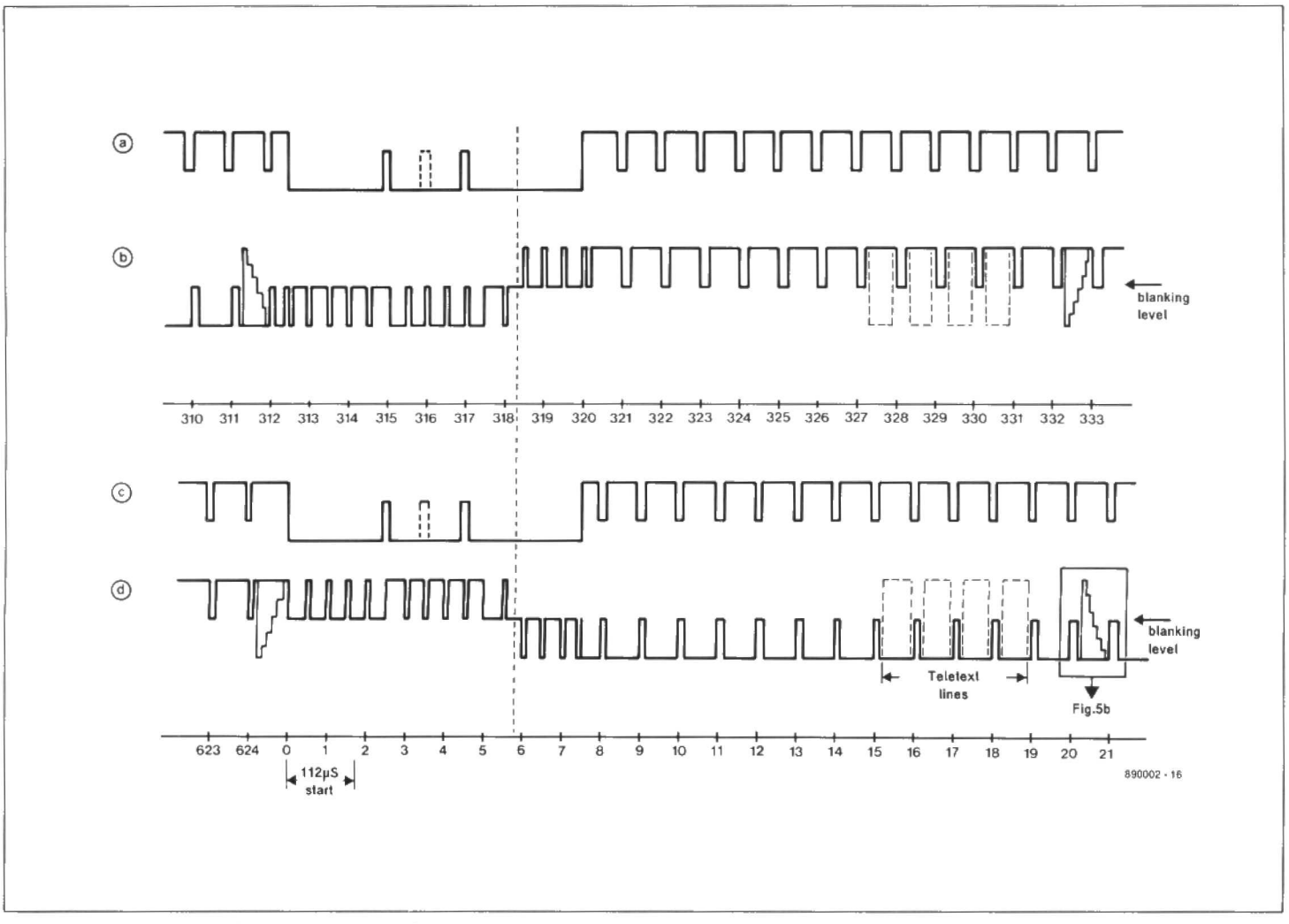


Fig. 6. Raster analysis of the decoded signal.

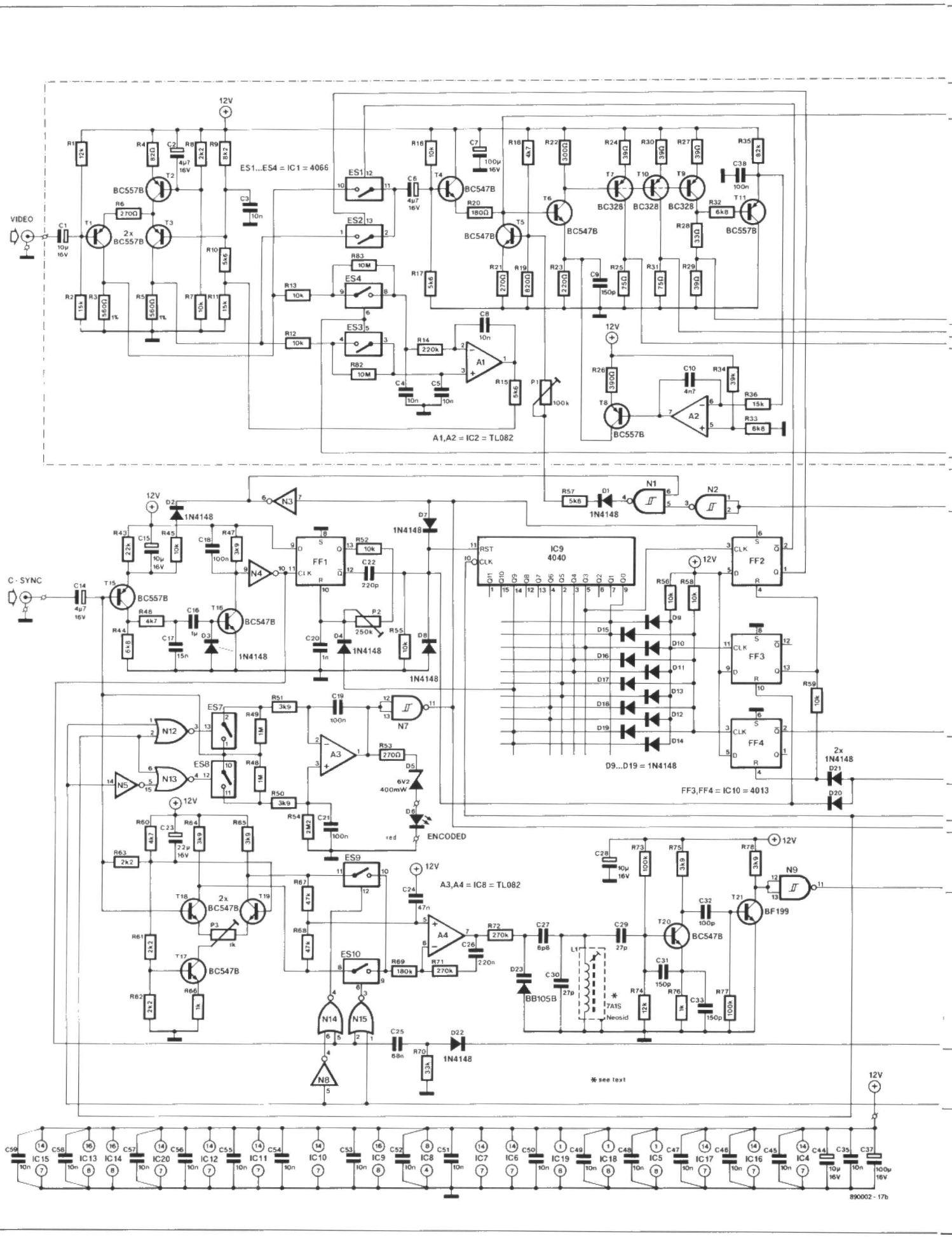
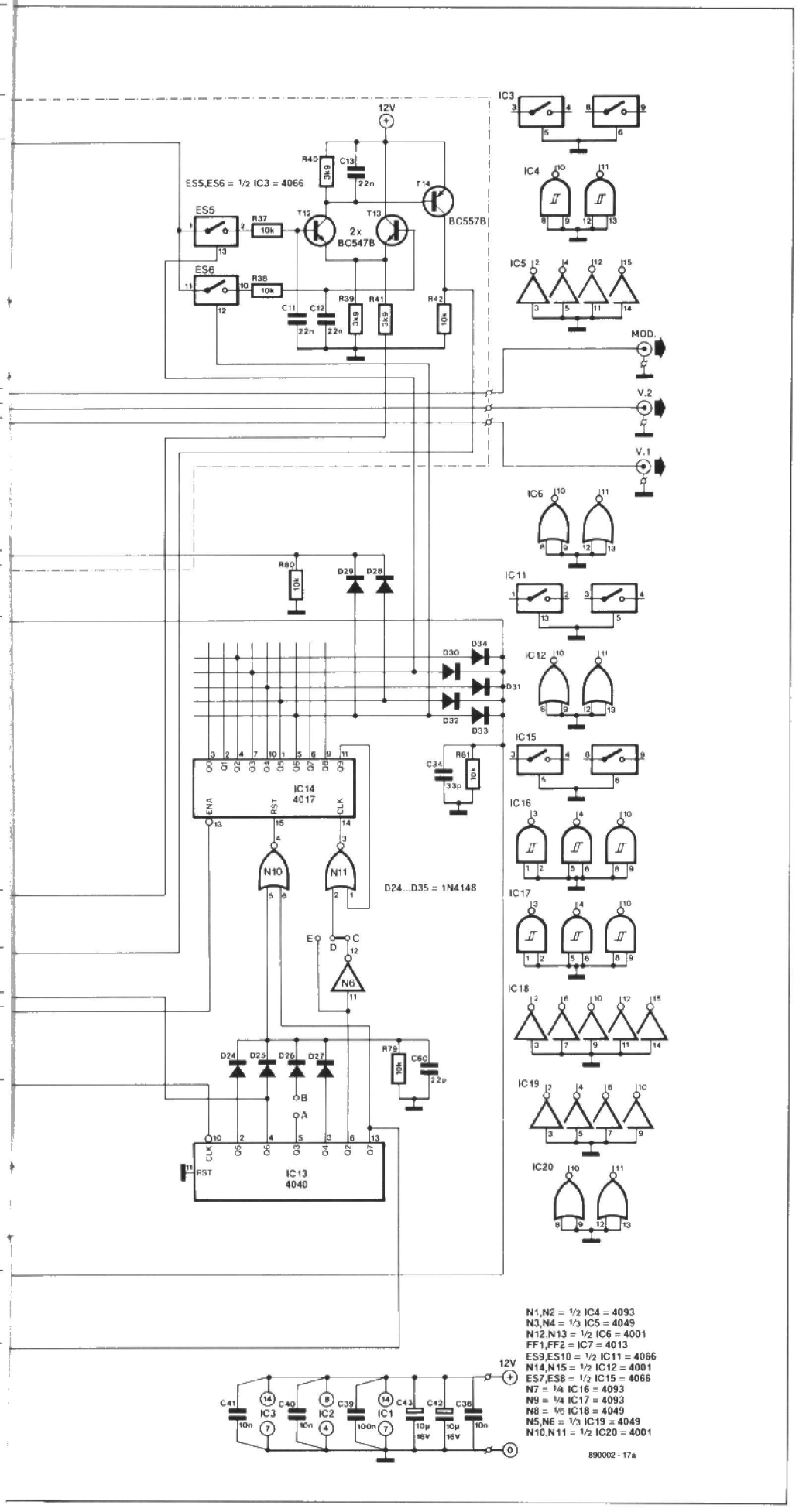


Fig. 7. The automatically switching ATN-Filmnet decoder is a remarkable combination of digital and analogue electronics. Even the multi-language Teletext service on Filmnet is retained! Wire links A—B and C—D/D—E serve to compensate phase shift in the baseband or unclamped-video signal supplied by the indoor unit.



ES4 sample both voltages during the blanking period. Opamp A1 filters and compares these samples, and generates an error signal that is fed to the second input of difference amplifier T1-T2. The blanking levels of the subsequent rasters (inverted and non-inverted) are thus held at a virtually equal level. Equal levels are important to avoid picture flicker in light-coloured areas (clouds!) in the top part of the TV picture. With this in mind, the use of close-tolerance resistors in positions R3 and R5 is logical.

Depending on the state of the previously described logic circuitry, either UR3 or UR5 is applied to buffer T4, which feeds the video signal to R20. This resistor passes a constant current of about 4 mA, ensuring that the video signal at the emitter of T4 is still undistorted when it is taken from the collector of T5. The required shifting up by 30% of the video signal is achieved by controlled lowering of the collector current of T5, so that UR20 drops. The resulting video off-set can be set to exactly 30% with the aid of preset P1.

Transistors T7, T10, T9 and T6 buffer the video signal, which is then ready for driving 75 Ω loads connected to two DC-coupled CVBS outputs, marked V.1 and V.2. A further output, marked MOD., may be used for driving a video modulator with an input impedance not lower than 500 Ω.

Construction

Since a ready-made PCB for this project is not available, the board has been designed single-sided (see Fig. 8) to avoid difficulties in etching and manual through-plating. The result is a fairly large board (29×13 cm) which may be cut in two to separate the video processor from the PLL plus logic circuitry. The 7.56 MHz c-sync receiver is built on a separate board (see Fig. 9) which may be installed permanently in the indoor unit.

Even expierenced constructors will need several hours to select, position and fit the components in place as shown by the component overlay (see Fig. 8). Construction is, none the less, entirely straightforward with a fair number of parts mounted vertically. IC sockets should be used in all positions.

VCO inductor L1 is made from 60 turns of 0.1 mm diameter enamelled copper wire (2 layers; closewound) on the white, ABS, former that comes with the Type 7A1S inductor assembly from Neosid. No attempt should be made to replace this inductor with a ready-made type, since its Q-factor and L-C ratio are critical. After winding and connecting the inductor, the cup core is positioned and secured with wax or glue (see Fig. 10). Screw the ferrite core into the former, mount the screening can, check

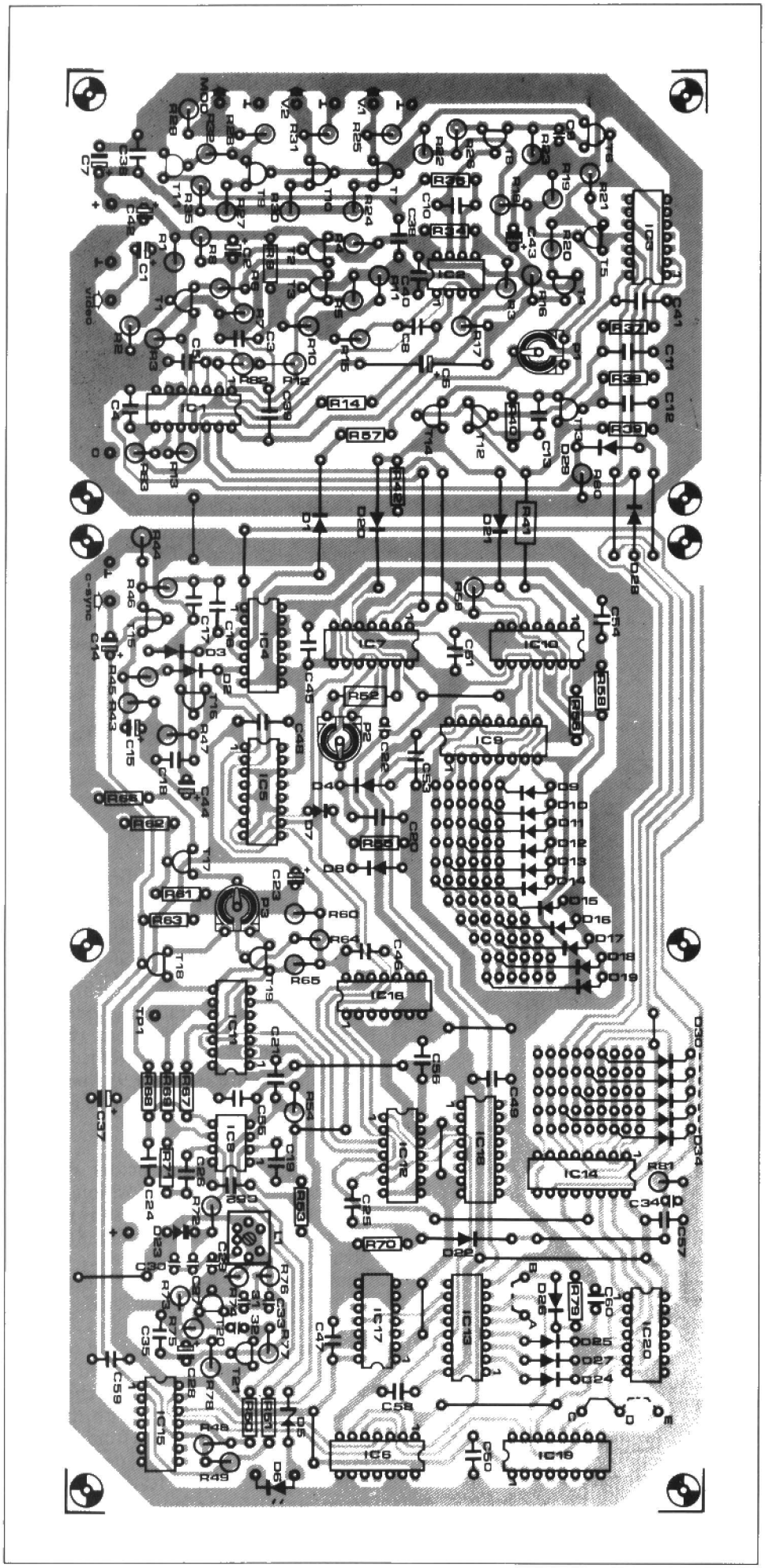


Fig. 8. The printed-circuit board for the decoder may be cut into two to separate the digital circuitry plus PLL from the video processor (PCB shown at 90% of actual size).

Parts list

Resistors (±5%):
R1;R74 = 12K
R2;R11;R36 = 15K
R3;R5 = 560R; 1%
R4 = 82R
R6;R21;R53 = 270R
R7;R12;R13;R16;R37;R38;R42;R45;R52;R55;R56;R58;R59;R79;R80;R81 = 10K
R8;R61;R62;R63 = 2K2
R9 = 8K2
R10;R15;R17;R57 = 5K6
R14;R72 = 220K
R18;R46;R60 = 4K7
R19 = 820R
R20 = 180R
R22 = 300R
R23 = 220R
R24;R27;R29;R30 = 39R
R25;R31 = 75R
R26 = 390R
R28 = 33R
R32;R33;R44 = 6K8
R34;R70 = 33K
R35 = 82K
R39;R40;R41;R47;R50;R51;R64;R65;R75;R78 = 3K9
R43 = 22K
R48;R49 = 1M0
R54 = 2M2
R66;R76 = 1K0
R67;R68 = 47K
R69 = 180K
R71 = 270K
R73;R77 = 100K
R82;R83 = 10M
P1 = 100K preset H
P2 = 250K preset H
P3 = 1K0 preset H

Capacitors:

Electrolytic capacitors are radial types unless otherwise noted.
Ceramic capacitors are 2.5 mm pitch.

C1;C15;C28;C42;C43;C44 = 10μ; 16 V
C2;C14 = 4μ7; 16 V
C3;C4;C5;C8;C35;C36;C40;C41;C45 to C59 incl. = 10n
C6 = 4μ7; 16 V axial
C7;C37 = 100μ; 16 V
C9;C31;C33 = 150p
C10 = 4n7
C11;C12;C13 = 22n
C16 = 1μ0; MKT
C17 = 15n
C18;C19;C21;C38;C39 = 100n
C20 = 1n0
C22 = 220p C23 = 22μ; 16 V
C24 = 47n
C25 = 68n
C26 = 220n
C27 = 6p8
C29;C30 = 27p
C32 = 100p
C34 = 33p
C60 = 22p

Inductor:
L1 = 7A1S (Neosid)

Semiconductors:
D1 to D4 incl.;D7 to D22 incl.; D24 to D34 incl. = 1N4148
D5 = zener diode 6V2; 0.4 W
D6 = red LED; 5 mm dia.

D23 = BB105B
T1;T2;T3;T8;T11;T14;T15 = BC557B
T4;T5;T6;T12;T13;T16 to T20 incl. = BC547B
T7;T9;T10 = BC328
T21 = BF199
IC1;IC3;IC11;IC15 = 4066
IC2;IC8 = TL082
IC4;IC16;IC17 = 4093
IC5;IC18;IC19 = 4049
IC6;IC12;IC20 = 4001
IC7;IC10 = 4013
IC9;IC13 = 4040
IC14 = 4017

Miscellaneous:
BNC sockets as required for inputs and outputs.
2 off 8-way IC sockets.
12 off 14-way IC sockets.
6 off 16-way IC sockets.
15 off PCB soldering pins.
PCB 890002-1 (not available ready-made through the Readers Services).

continuity of the winding at the base pins, and solder the assembly in place. For optimum stability of the circuit, the ceramic capacitors in the 4 MHz VCO should be low thermal-coeffient (NP0) ceramic types, marked with a black dot or bar at the top. Also make sure that the core in L1 is secure in the former.

The default wire-link configuration is as shown in the circuit diagram of the decoder: A—B not fitted; C—D fitted.

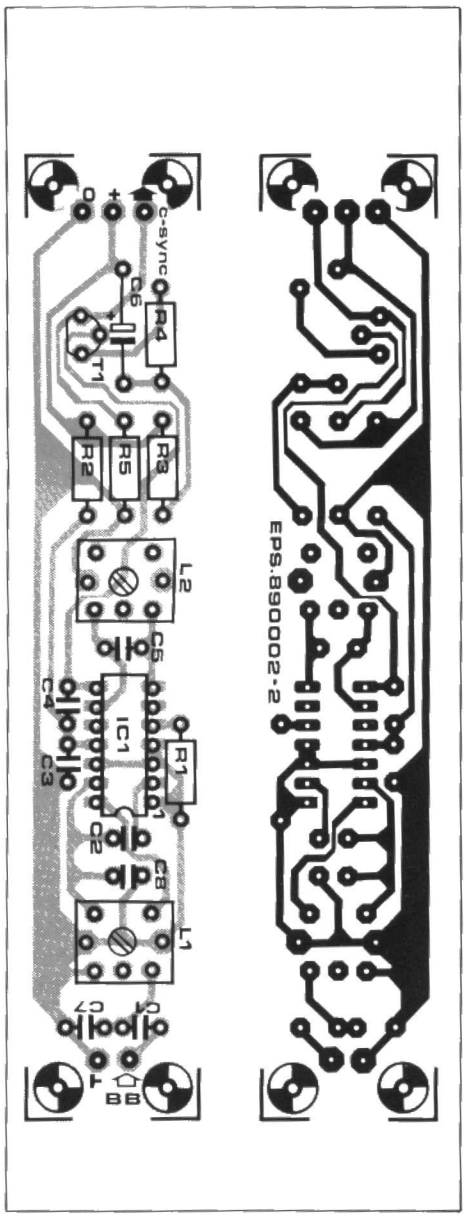
Construction of the sync receiver on the PCB shown in Fig. 9 is a matter of routine, and requires no further discussion. In view of the relatively high frequencies involved (0 to 8.5 MHz), the connection between the baseband input (BB) and the relevant output on the indoor unit should be made in thin, 50 or 75 Ω, coaxial wire and BNC sockets and plugs.

Connecting-up and alignment

The sync receiver, decoder and indoor unit are interconnected as shown in Fig. 11.

As may have been noted already from the earlier circuit descriptions, the operation of the decoder hinges on the phase shift introduced by the sync receiver. No attempt should, therefore, be made to modify this module, or replace it with another design. Along the same lines, the decoder will not work properly when driven with a video signal that has been clamped or filtered in any type of anti-dispersal circuit. The technical specification supplied with your indoor unit should indicate whether a suitable signal is available for driving the decoder. If necessary, an unclamped-video and/or baseband output will have to be post-installed by the user himself.

In some cases, however, a separate baseband output may not be necessary because the c-sync receiver is so sensitive that it can be driven from the unclamped-video output also (post-de-emphasis connection).



Parts list

Resistors (±5%):
R1 = 4K7
R2 = 100R
R3 = 680R
R4 = 270R
R5 = 330R

Capacitors:
C1 = 4p7
C2;C8 = 22n ceramic
C3 = 100n
C4 = 1n0 ceramic
C5;C7 = 82p
C6 = 47μ; 16 V axial

Semiconductors:
T1 = BC557B
IC1 = TBA120S (do not use -T or -U suffix)

Inductors:
L1 = KACSK3893A (Toko)
L2 = KACSK586HM (Toko)

Miscellaneous:
PCB Type 890002-2 (not available ready-made through the Readers Services).

Fig. 9. This narrow PCB holds the TBA120S-based sync-receiver.

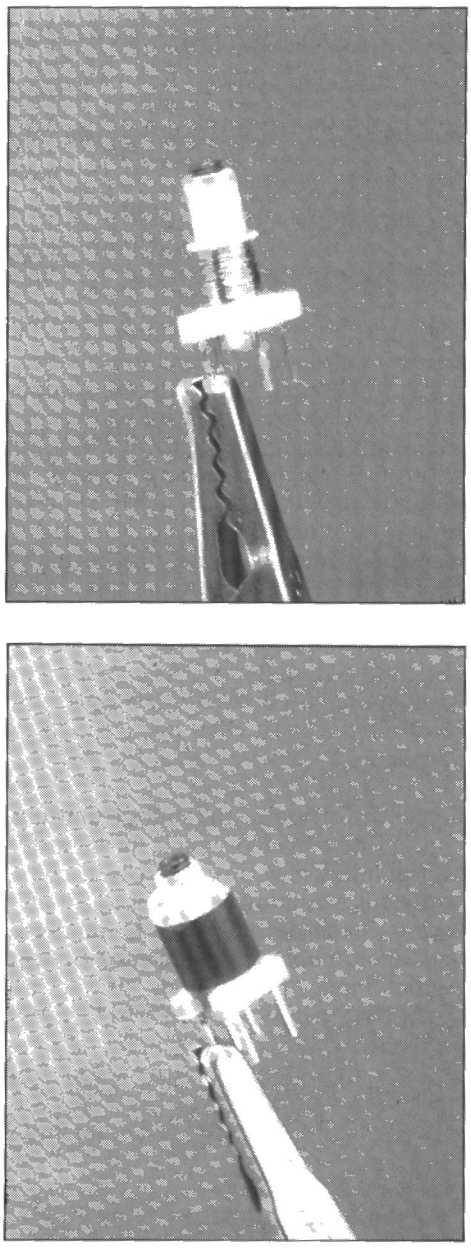


Fig. 10. Home-wound VCO inductor L1 before (above) and after (below) fitting the cup core. The inductance of L1 is about 22 μH.

In the *Elektor Electronics* Indoor Unit (Ref. 1), the signals for driving the decoder are available as follows:

Baseband: output pin 7 of RF module (86082-1) to input of sound/vision/PSU module (86082-2);
Unclamped video: pin 8 of IC_3 (NE592 video amplifier) on sound/vision/PSU module (86082-2).

The unclamped-video input of the decoder has an input impednce of about 5 kΩ. If the video signal from the indoor unit is carried over a relatively long coax cable, it is recommended to fit this input with a 75 Ω termination resistor to ground. In all other cases, a 470 Ω preset should be fitted as shown in Fig. 11b to enable a reduction of the input signal to about 1 V_{pp}. Driven with this input level, and terminated in 75 Ω, the video processor in the decoder provides an amplification of 1.25. During setting up with an oscilloscope, a 75 Ω termination resistor *must* be fitted at the output of te decoder.

Signal distortion in the indoor unit and poorly filtered video signals on some TV transponders may, in some cases, cause erroneous actuation of the PLL. To prevent this, the decoder may be rendered inactive *manually* by short-circuiting its c-sync input to ground. If at all necessary, this is simplest to arrange with a switch as shown in Fig. 11b (note that the output of the sync receiver is short-circuit resistant).
The highly non-linear demodulation characteristic of some indoor units may cause noticeable display flicker in white areas of the upper part of the picture. Obviously, the decoder can not be blamed for this, and there is probably no other way of remedying this effect than to call in the assistance of your TVRO dealer.
A prototype of the decoder gave excellent results in conjunction with the widely used Connexions CX8520R indoor unit.

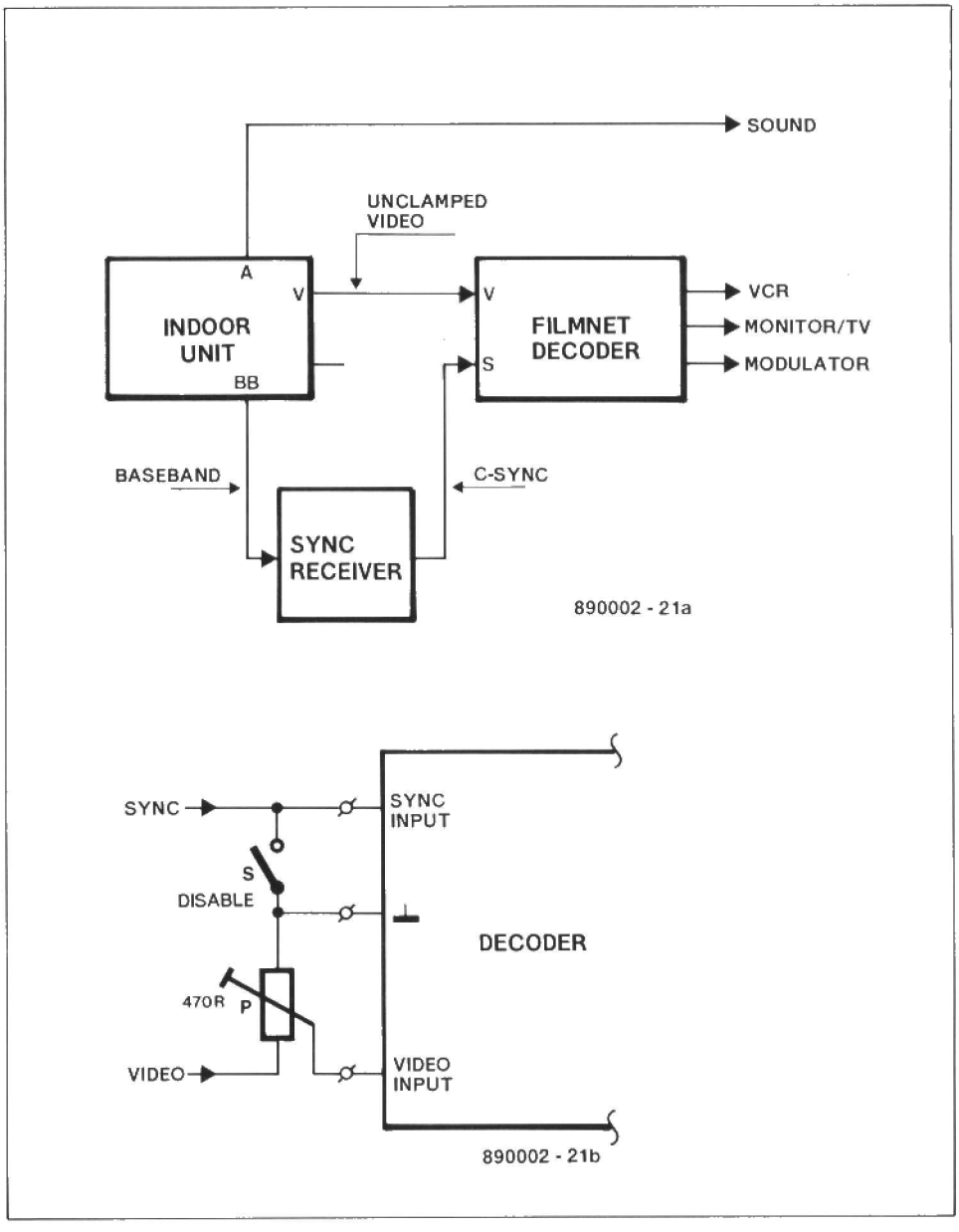
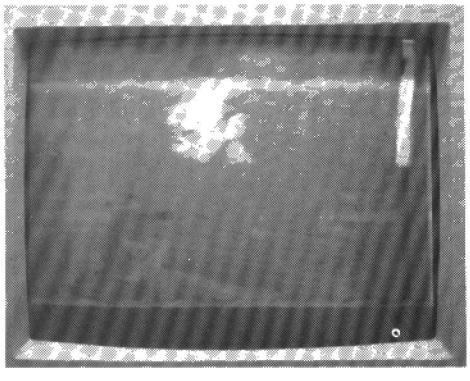


Fig. 11. Connections between indoor unit, sync receiver, decoder and TV set or monitor. In some cases, the c-sync receiver may be connected to the unclamped-video output, obviating the need for a baseband output.



Before.....

and after decoding...

Setting up

For the following description it is assumed that the completed decoder and sync receiver have been connected as shown in Fig. 11, and that a frequency meter and an oscilloscope are available.

First, the pulse receiver is aligned:

- Set the scope to line-sync triggering, and connect it to the c-sync output of the receiver module. Align L_1 and L_2 for minimum noise and highest undistorted amplitude of the output pulses (be sure to steer clear of the FSK data channel at 7.2 MHz). The added parallel capacitors across the Toko inductors have been dimensioned such that resonance at 7.56 MHz will almost always occur with the core turned in about half-way the former.

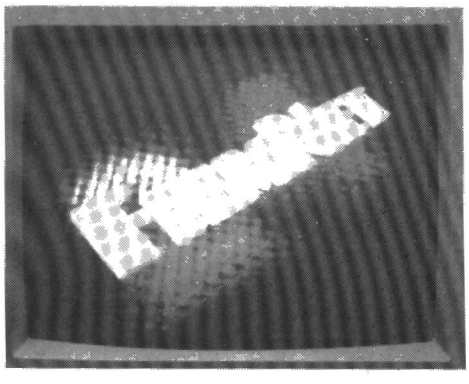
Then it is time to concentrate on the main decoder board:

- Set all three presets in de decoder to the centre of their travel.
- Check the presence of the c-sync pulses at the base of T_{18}.
- Short-circuit the c-sync input to ground, or close external switch S.
- Connect the frequency meter to pin 1 of IC_{13}, and adjust the core in L_1 for 4.00 MHz.
- Use the scope to check that the waveform at TP1 is a 15,625 Hz, rectangular, signal. Adjust the balance preset, P_3, for *minimum* amplitude of this signal. Open switch S and check the

displayed waveform against that shown in timing diagram Fig. 5e. The 'ENCODED' LED, D_6, will probably light at this stage.

- Align P_2 for the required 112 µs delay: connect the scope to one of the decoder outputs, and set it to v-sync triggering. Adjust P_2 until all pulses in the rear-porch equalizing period point downwards (see also Fig. 6).
- Adjust P_1 for a blanking level that is equal to, or slightly lower than, the black level in the video information. The picture is now stable and decoded!

Note: two approximately 1 µs long, positive, pulses are generated adjacent to the line-sync pulse. These pulses must be present in a correctly decoded ATN-Filmnet signal. Wire links D—E and/or A—B may be fitted to correct a too wide pulse to the left of the sync pulse. The effect is caused by additional signal delay in the sync receiver, if this has a too narrow bandwidth. Some experimentation and fine-tuning of the inductors in the c-sync receiver may be necessary to get equally wide pulses. The pulses must not, under any circumstances, be negative-going, because this makes correct decoding impossible.



Finally, the completed video processor board may be mounted upside-down on the main decoder board with the aid of PCB spacers.

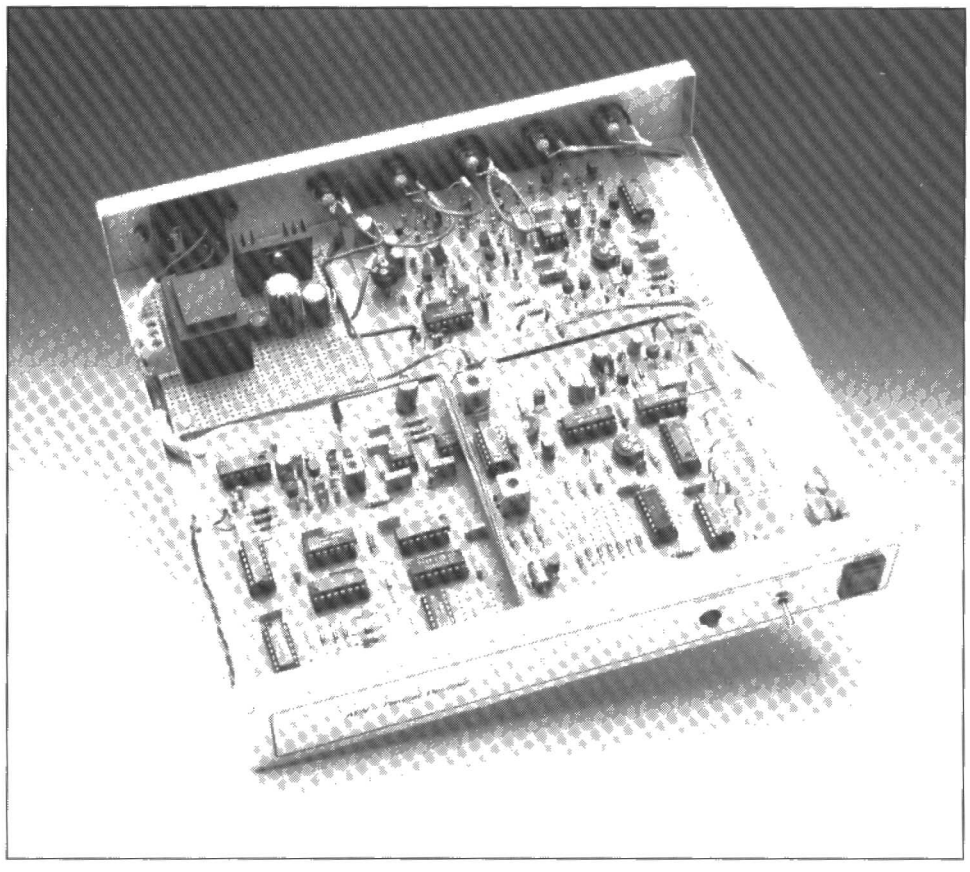
The decoder must be fitted in a metal enclosure, and is conveniently powered from a standard, 7812-based, 12 VDC supply, or one available in the indoor unit. Current consumtion with the 'ENCODED' LED on is less than 200 mA. ◀

Reference:

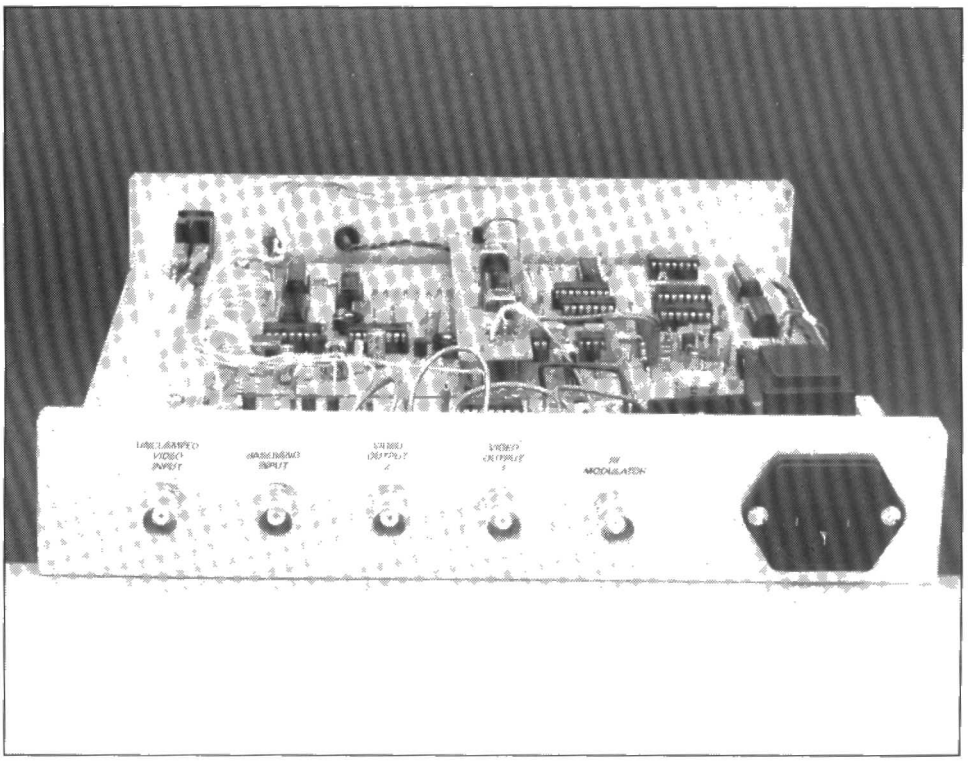
1. Indoor Unit for Satellite TV reception. *Elektor Electronics* October/November 1986; January 1987.

Editorial Note:

As already stated in this article, the scrambling system employed by ATN-Filmnet allows a number of technically different encoding modes, some of which may not be handled correctly by the present decoder. Mode-switching by ATN-Filmnet is irregular with operational periods of 2 to 8 months. Technical details of future scrambling modes are not known at the time of writing (January 1989). The prototype of the decoder described here has been in use since early August 1988. Information on the conversion of this circuit for use with cable systems is not available.



A look inside the completed prototype of the ATN-Filmnet decoder. Since it was used for experimental purposes, the c-sync receiver was mounted in the decoder enclosure, rather than in the indoor unit. Also note the simple 12 V supply in the top left-hand corner of the box.



Constructors of this project are advised that the artwork (on paper) for PCBs 890002-1/2 is available free of charge — details on ordering are given on the Readers Services page in this issue.

DESIGN IDEAS

The contents of this column are based solely on information supplied by the author and do not imply practical experience by *Elektor Electronics.*

COUNTER WITHOUT COUNTER

Under this paradoxical title we present a design idea for a versatile counter concept that uses an EPROM instead of the expected counter chip.

by N. Körber

The circuit described here can be configured as an up- or down-counter from 0 to 99 in BCD or 8-bit binary mode, with reset, preset and enable inputs available. All control inputs are digital compatible, allowing the user to define his own control hierarchy. Moreover, the control inputs may be active high or active low.

The counter is actuated by the positive transitions in the clock signal, and handles input frequencies well into the MHz-range. All inputs and outputs are TTL-compatible. The counter is so remarkable because its features and versatility are achieved with only a handful of commonly available components.

The Moore system

From a point of view of information technology, the present counter is similar to a so-called synchronous transforming Moore circuit. The indication *synchronous* has to do with the clock signal and the way in which the inputs are driven. A Moore circuit is a logic unit that processes input parameters x and internal conditions z to produce output states y. Each condition is associated with only one output state. As a result of input parameters and internal conditions, the Moore circuit steps through a number of states. The system not only uses currently available information, but also information acquired from past operations, whose system conditions have been recorded. A clock signal is required to switch the system to the next state.

In practice

A real Moore system is composed of a switching network and a memory. In the case of the present counter, the input parameters are the data applied to the

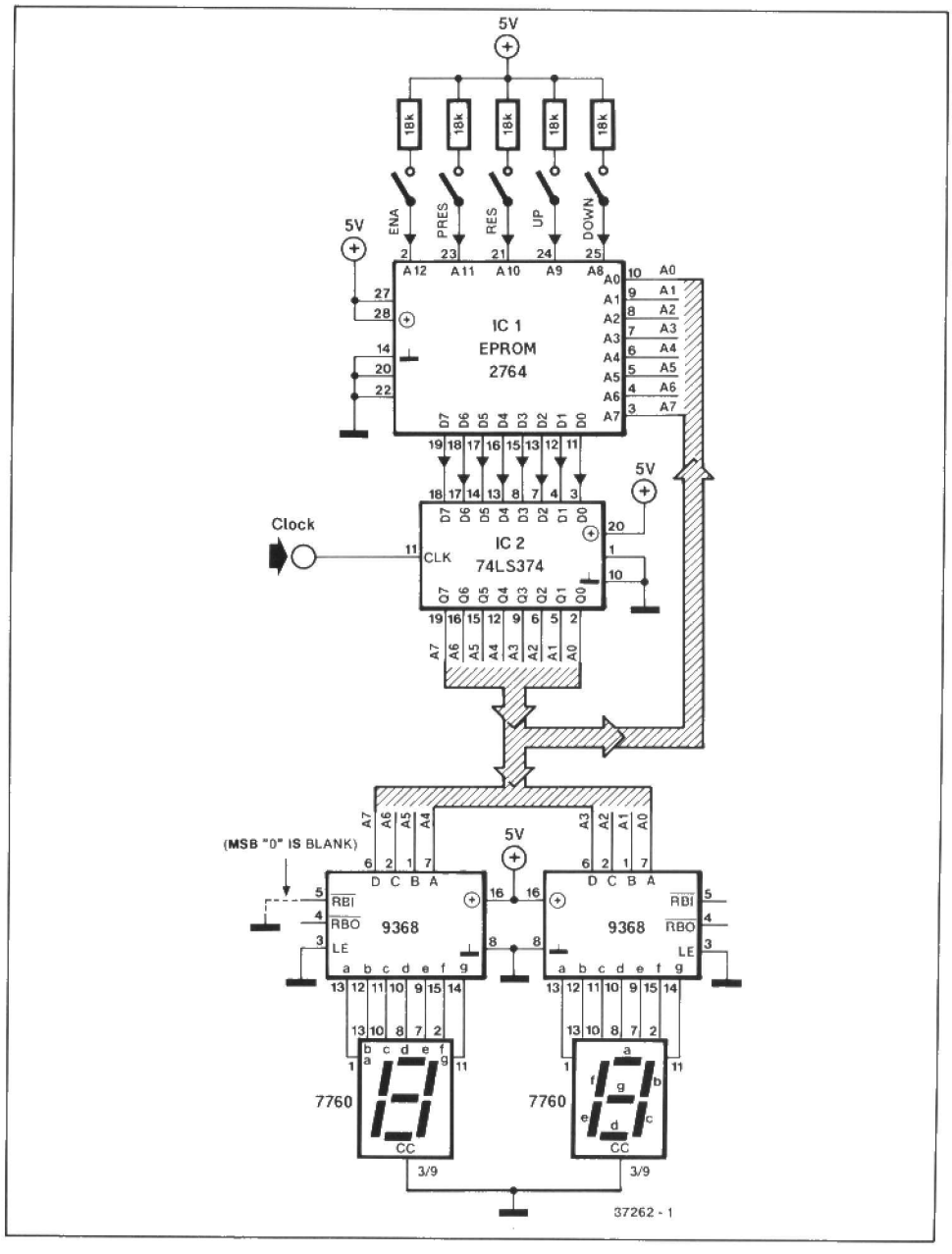


Fig. 1. Basic design of an EPROM-based counter.

control inputs. These are connected to an EPROM, which combines these data with the current conditions, to generate a system state. This state is copied into a latch (IC_2 in the circuit diagram), and so becomes the *current state*. In principle, output state *y* would then have to be generated with the aid of a further switching element. This procedure is not needed here, however, by virtue of the EPROM, which, if properly programmed, ensures that the output value (i.e., the counter state) is exactly the value that corresponds to the current state.

The operating principle of the circuit discussed here is fairly complex, but may be explained with the aid of a hypothetical circuit, based on an EPROM Type 2764 addressed between 0000 and 1FFF, that serves to count seconds pulses applied to the clock input by an external circuit.

First consider the basic timing of the events that take place in the circuit. Because switch ENA (enable) is connected to address line A12 of the EPROM, it divides the available memory capacity in two equal halves. Each of these is, in turn, subdivided in two by line A11 (switch PRESet), and again in two by the RESet switch connected to A10. For the actuation of the RESet switch to cause the displays to indicate 00, it is necessary that all memory sub-partitions addressed with A10=1 (for example, 0000 to 03FF, or 0BFF to FFFF) contain data 00.

With this in mind, and returning to the seconds counter, it is clear that 00 should be displayed when RESet is actuated. To achieve this, data available at outputs Q0 to Q7 of octal bistable IC_7 must cause the display drivers Type 9368 to drive those display segments that together form a 0.

A positive pulse transition at the clock input of the 74LS374 causes the logic state applied to each data inputs, D_n, of the chip to be copied to the corresponding output, Q_n. Assuming that the circuit is to function as a down-counter, EPROM address line A9 is made logic high by closing switch DOWN. In the 1 KByte memory area adressed, 512 bytes may be programmed such that the displayed value is decremented. Care should be taken to ensure a correct programmed sequence, since 59 must be displayed once the counter has been started.

The circuit diagram of Fig. 1 clearly shows the sub-units of the counter: the external controls in the form of switches, the EPROM, the latch circuit, and the display drivers for two 7-segment LED displays. The control parameters of the counter, ENAable, RESet, PREset and DOWN, and the current state, are applied in parallel to the address inputs of the EPROM. The EPROM uses the address so obtained to produce information on the next state. This information is made available on data outputs D0 to D7, and, a little later, on outputs Q0 to Q7 of the latch, from where it is sent to the displays. This process starts with each rising edge of the clock signal.

Table 1. EPROM programming example for a 60-state cyclic up/down counter.

Function:	RESET
ADDRESS	DATA
$0400 – 1FFF	00

Function: COUNT UP		Function: COUNT DOWN	
ADDRESS	DATA	ADDRESS	DATA
$1100	01	$1200	59
1	02	1	00
2	03	2	1
3	04	3	2
4	05	4	3
5	06	5	4
6	07	6	5
7	08	7	6
8	09	8	7
9	10	9	8
A	*	A	*
B	*	B	*
C	*	C	*
D	*	D	*
E	*	E	*
F	*	F	*
10	11	10	9
11	12	11	10
:	:	:	:
:	:	:	:
$1159	00	$1259	58

* don't care

Table 2. EPROM programming example for a decimal up/down counter.

Function	Address							EPROM contents	
	A12	A11	A10	A9	A8	A7 à A0		D7 à D0	
	ENA	PRES	RES	DOWN	UP	state z		resulting state	
	1	*	0	0	1	0000	0000	0000	0001
Count up	1	*	0	0	1	a	b	a	b+1
	1	*	0	0	1	a	1001	a+1	0000
	1	*	0	0	1	1001	1001	0000	0000
	1	*	0	1	0	0000	0000	1001	1001
Count down	1	*	0	1	0	a	0000	a–1	1001
	1	*	0	1	0	a	b	a	b–1
reset	*	*	1	*	*	****	****	0000	0000
	0	0	0	*	*	i		i	
Preset	0	1	0	*	*	****	****	j (dont't care)	
all other bit combinations						i		i	

* = don't care

Programming the EPROM

The actual contents of the EPROM depend on the application of the counter circuit, and must, therefore, be provided by yourself.

The 8 Kbyte EPROM is perhaps best thought of as 8 blocks of 256 bytes. Each of these blocks is addressed by applying a particular (model-) dataword to the address inputs. When the control parameters remain umchanged, only the information applied to inputs A0 to A7 determine the output state. The changes from one state to another are a function of the preprogrammed contents of the relevant block. If, for example, RESet is pressed, the change to the next state results in the displays reading 00.

As a practical programming example, Table 1 lists the EPROM contents for a down-counter and an up-counter with 60, cyclic, states — the seconds counter discussed above. For a similar counter with, say, 100 states, the memory locations up to $1198 have to be loaded, with $1198 and 1199 reading 99 and 00 respectively (UP function). Similarly, the down-counter starts at $1200 with data 99, and 98 at $1299. Table 2 shows a further example of how the EPROM may be programmed: in this case, a two-digit decimal up/down counter is obtained.

THE DIGITAL MODEL TRAIN — PART 2

by T. Wigmore

The second part in the series describes a locomotive decoder that is constructed in surface-mount technology. In conjunction with the associated digital control system, it enables up to 80 trains to be controlled independently. The associated control system will be described in a future article, but in the mean time the present decoder may be used with the Marklin digital system or any two-rail model track.

The use of surface-mount techniques (SMT) makes it possible to construct a locomotive decoder from standard components that is compact enough for fitting into a locomotive. These techniques are undoubtedly new to many readers, but this article will show that there is no real mystique about them.

The present decoder enables both a.c. and d.c. locomotives to be controlled independently of one another. In its simplest form, it is suitable for use on tracks with a centre rail (Marklin or Trix, e.g.) or with an overhead power line. The addition of the two-rail adaptor discussed later in the article enables the decoder to be used with other model railway systems. It should be noted, however, that although the decoder is compact, it can not be fitted in locomotives smaller than HO.

In Marklin stock, the space for the decoder board is ensured, because the change-over relay may be removed. This is possible, even desirable, since the decoder enables a change of direction (and the consequent switching of the head and tail lights) to be effected electronically.

As already stated, the decoder may be used with a.c. as well as d.c. systems. It is thus possible to convert a d.c. locomotive for use on an a.c. track by providing it with a slip contact and the present decoder.

In principle, it is also possible to use a Marklin locomotive on a track of different manufacture. If, however, that track is a two-rail system, the wheels of the locomotive must be electrically separated and provided with appropriate contacts. Moreover, if a two-rail track is used, the adaptor described later is also required. Although possible, this conversion is, therefore, in general not practicable.

The two-rail adaptor is also constructed in surface-mount technology and may be mounted on to the decoder. The resulting sandwich is only 2.5 mm thicker than the decoder board by itself. The use of the two-rail adaptor makes the locomotive decoder independent of the polarity of the supply and data connections. As an aside, this also solves the eternal problem of reversing loops.

- independent control of up to 80 locomotives
- may be driven by Marklin HO system or Elektor Electronics Digital Model Train System
- suitable for a.c. and d.c. locomotives
- suitable for three-rail system or, with optional adaptor, for two-rail systems
- motor current max. 1 A (peak 1.5 A)
- protected against thermal overload
- speed controlled in 16 steps
- automatic change-over of independently lit head and tail lights
- lamp voltage 10 V or 20 V as required
- optional: memory from external buffer capacitor
- compact dimensions through surface-mount technology:
  35 × 24 × 7,5 mm (decoder only)
  35 × 24 × 10 mm (with two-rail adaptor)

Table 2. Technical data of the locomotive decoder.

Compatibility

Apart from the possibility of its use in a large variety of locomotives, the decoder may be operated with a number of control systems. In this context, it is perhaps of interest to know that it was designed originally and solely as part of the Elektor Electronics Digital Multi-train System which will be described in this series of articles. However, with a few simple changes (such as the baud rate), it also proved usable with the Marklin digital HO system. It is, of course, important to differentiate between the Marklin decoders and the present one.

In view of the required compactness of the decoder, the spare function offered by Marklin has had to be sacrificed in the present decoder (see Fig. 14). Marklin uses the lowest speed step (binary 1000) for reversing, assuming that this step will not be used in practice, since the motor does not operate smoothly at this (average) low voltage. To use this voltage for reversing the direction of travel, it has to be decoded and then used as the clock signal for a bistable. In the present decoder, this

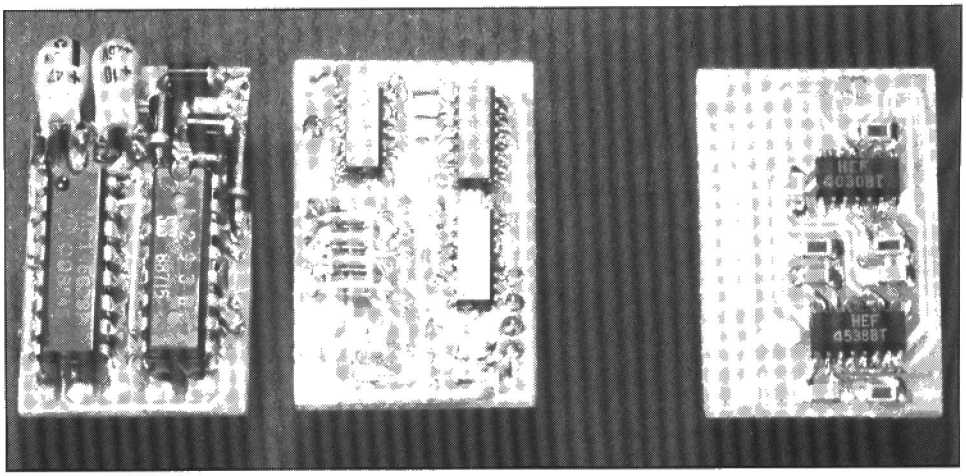


Fig. 11. The locomotive decoder is populated with mainly conventional components at the component side and with surface-mount ones at the track side to give a compact unit. At the right of the picture is the single-sided PCB for the two-rail adaptor that uses only surface-mount components.

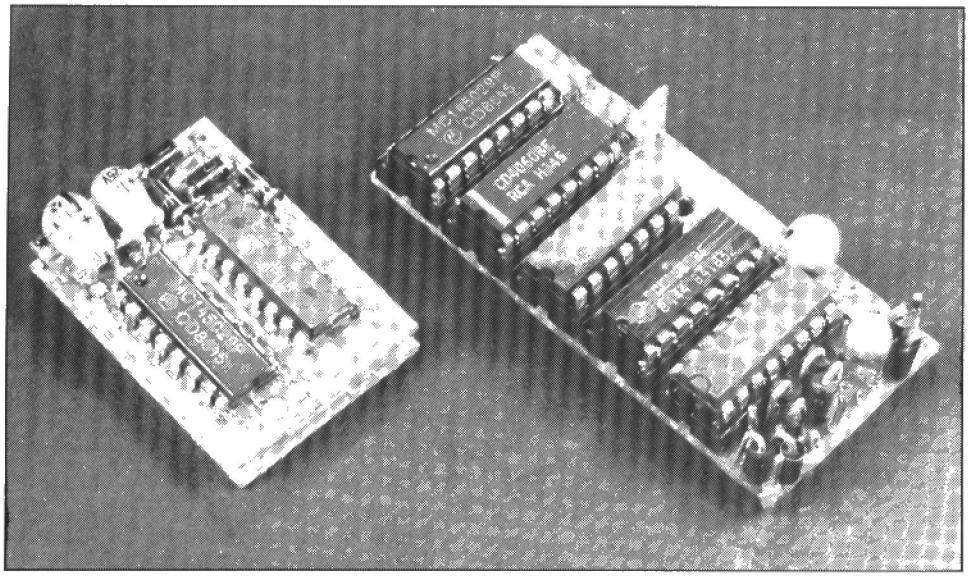


Fig. 12. At the left the prototype locomotive decoder and two-rail adaptor sandwiched together. At the right a locomotive board constructed with conventional components, which is evidence of the space saving afforded by surface-mount techniques.

would have required two additional ICs, which would have made the board too large. Fortunately, in most cases the spare function is not required anyway. Where it is needed, there is no alternative to using a Marklin decoder.
Note that if the present decoder is driven via Control 80 of the Marklin system, the spare function is used for reversing. A more important difference between the Marklin decoder and ours manifests itself if locomotives converted for use in a digital system are run on conventional (non-digital) tracks. The Marklin decoder may be used with conventional control systems, i.e., the speed may be varied according to the amplitude of the (alternating) supply voltage and the direction of travel may be changed by an over-voltage pulse of not less than 24 V. The present decoder does not offer these facilities: in fact, a 24-V pulse (in practice, this value is normally considerably higher) would probably put paid to the power stage. It is therefore strongly recommended to use the decoder only with digital tracks.
Furthermore, the present decoder does not support Fleischmann's digital FMZ system nor that from Trix. However, locomotives in those systems (and most others) may be converted with the present decoder to make them suitable for use in multi-train set-ups. It will then depend on the rail system whether, apart from the locomotive decoder, the rail adaptor is also required.

Start at the beginning: the rails

The most important difference between a digital model railway and a conventional one is that in the former, just as in real railways, the rails carry a constant voltage. To prevent that in these circumstances all locomotives on the track travel along at full speed, they are all fitted with a decoder and a speed controller. In other words, as in real life, the speed of the locomotive is varied on board, just as if it had an engine driver. The instructions to the "engine driver" emanate from a central control, which in turn is controlled by a number of independent drive units or a computer.

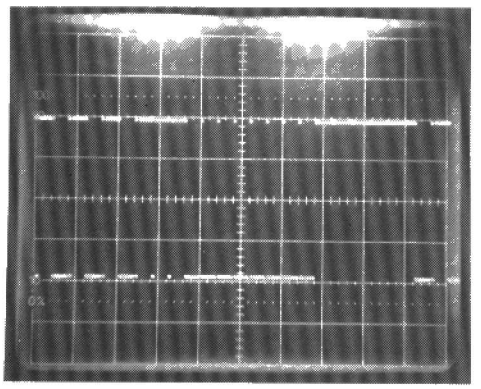


Fig. 13. The track voltage in a digital model railway systems is switched between −20 V and +20 V to ensure that the control instructions reach the locomotives via the rails in a serial data format. The locomotive power is obtained by rectifying this alternating voltage.

The instructions from the central control are transmitted to the locomotives by switching the supply voltage between +20 V and −20 V. The voltage on the rails is thus an alternating one, but it has a d.c. component whose value depends on the transmitted data.
Each period contains 18 "marker" pulses; each of the nine pairs of pulses defines a bit with three possible states: 00=logic 0; 10=logic indeterminate; 11=logic 1. In this way, 9-bit words are formed: the first four are interpreted by the decoder as address and the other five as data. The logic indeterminate state is used only for forming addresses; the five data bits use only logic 0 and logic 1.
Not only locomotives, but also turnouts (points) and signals may be controlled via the rails. Normally, locomotives are addressed constantly so that they exhibit real-time behaviour. The response time of the system becomes gradually longer as more locomotives are taken into use. An added advantage of the constant voltage on the rails is that permanent lighting of the train is possible without any difficulty. This applies, of course, also to the head and tail lights, even when the train is at standstill.

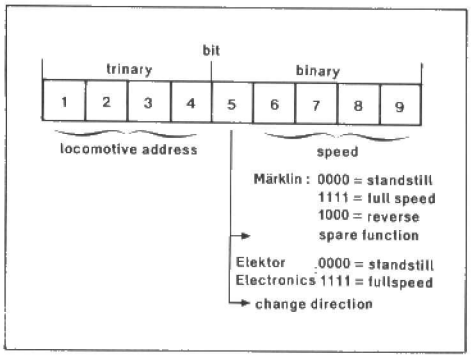


Fig. 14. The data bytes for the locomotives consist of nine bits. The first four bits form a trinary locomotive address. The other five are data that enable direction, speed and — in the Marklin system — a spare function to be controlled. One data byte is 3.8 ms long.

Block diagram

The operation of the locomotive decoder may be seen from the block diagram in Fig. 15. The rail voltage is full-wave rectified to create a supply for the power stages. Since the rail voltage is a square wave, the resulting d.c. is very pure, i.e., it has virtually no ripple. A lower direct voltage for the logic circuits is derived from the supply for the power stages.
The serial data are translated by a special decoder. These data are transmitted direct by the 'red' power line in three-rail systems or processed by the two-rail adaptor in two-rail systems. The trinary address part (first four bits) is compared with the address set on the decoder. If the two match, the next five data bits are accepted immediately. When the same five data bits have been received twice in succession, they are accepted as true and placed in the output latch.
Four of the five available data bits are used for operating the 16-step speed control; the fifth determines the direction of travel.
The speed is set with the aid of a digital pulsewidth modulator (PWM). The modulator consists of a four-bit counter with oscillator and a four-bit comparator. The counter (port A of the comparator) runs constantly. The four bits of the speed control are present at port B. Depending on the number at port B, the duty factor of the output signal varies between 0 and 15/16 at a frequency that

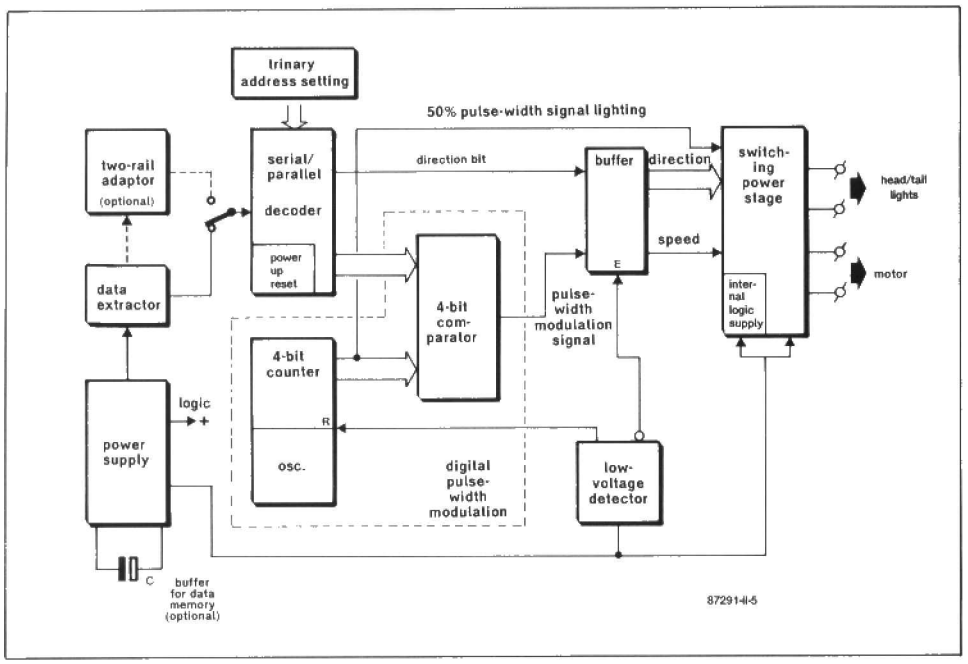


Fig. 15. The block diagram of the locomotive decoder.

is 1/16 of the counter frequency.
The PWM signal drives the output stage. Between this stage and the motor there is a fullwave rectifier. The polarity of the resulting direct voltage depends on the direction bit. This bit also serves to change over the head and tail lights that are driven by two half-wave circuits.
The lighting voltage may, if desired, be halved with the aid of a square-wave signal.
An undervoltage detector completes the set-up. If the supply voltage drops below a certain value, for instance, because the locomotive is travelling over an unpowered length of track, all signals are disconnected from the power stage and the logic circuits are set to the low-power state. In this state, the logic circuits are able to store the last received data for a short time, thanks to an optional external buffer capacitor. When the supply voltage recovers, the locomotive travels on at the last set speed.

Circuit description

In the circuit diagram of Fig. 16, the data decoding is carried out by IC_1, an MC145029 of the same family as the MC145027 used in the turnout and signal decoder described in Part 1 of this series. The significant difference between these two circuits is that in the former bit 5 is a data bit, while in the latter it is an address bit.
With the aid of wire links, a locomotive address may be set at address inputs A_1-A_4: more about this under 'construction'.
Network R_1-C_1 sets the baud rate of the decoder as required for the locomotives, while R_2-C_2 serves to detect the intervals between the data bytes.

Four of the data bits are fed to the four-bit comparator; the fifth, which, owing to N_1, is also available in inverted form, is used to change over the direction of travel and the lights via N_3, N_4 and the power stage. The counter with integral oscillator, IC_2, is designed so that the frequency of the MSB (Q_6 in this case) is about 140 Hz, which is also the frequency of the PWM signal (output of IC_3). This frequency was chosen because it will not cause undue problems owing to the self-inductance of the motor: higher frequencies may limit the motor current.
The power stage, IC_5, is a Type L293 from SGS. This chip contains four half-wave circuits, of which two may be combined into a full-wave bridge for bipolar motor control. The other two are used for the head and tail lights; these may therefore be switched relative to either earth or the positive supply line.
Gate N_2, R_6 and R_7 form the undervoltage detector. If the supply voltage

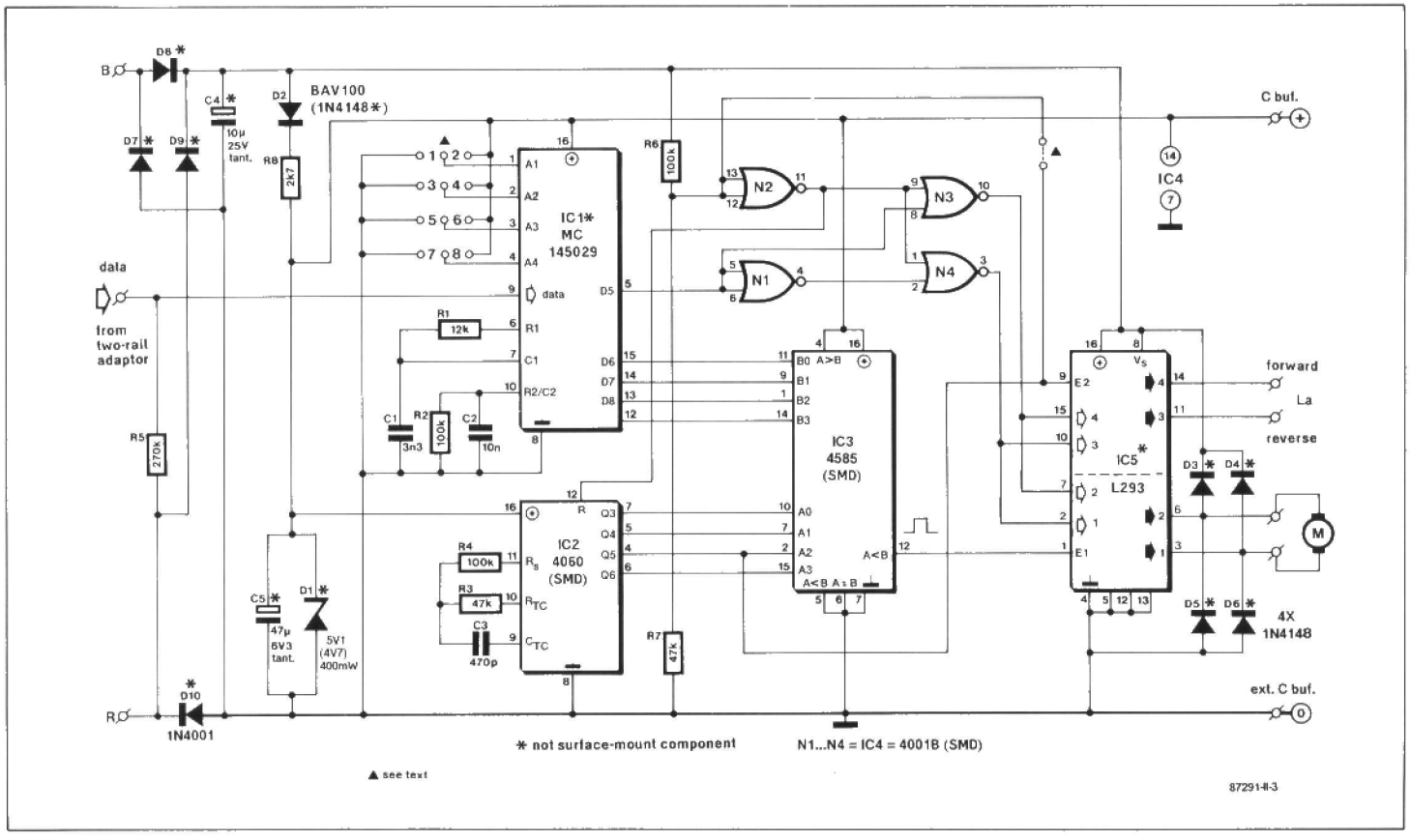


Fig. 16. The circuit diagram of the locomotive decoder.

drops below 8 V the potential at junction R_6-R_7 is interpreted by N_2 as a logic 0. This causes the reset input of the counter to become active, and this results in the PWM signal going low and the internal oscillator being stopped, which limits the current consumption.
At the same time, the remaining inputs of IC_5 are made logic 0 via N_3 and N_4. This is necessary to protect the chip (since its power supply is cut off) and to limit the current provided by the logic circuits.
The supply for the logic circuits in IC_5 is derived direct from the main power supply, because these circuits draw a fairly large current. When the main supply is present, the potential at junction R_6-R_7 is limited by the clamping diodes on board N_2 to a value that is slightly higher than that of the supply voltage for the logic circuits. If required, the E_2 input of IC_5 may be connected direct to this junction. In that case, virtually the full supply voltage is available for the lights. Since that voltage is fairly high (20 V), the E_2 input is fed with a 280 Hz square wave, which causes the effective voltage for the lights to be reduced to 10 V.
The main supply is obtained by full-wave rectification in D_7-D_{10} of the a.c. on the rails. Capacitor C_4 ensures continuity of the supply during the zero crossings of the rail voltage and blocks the counter emf generated by the self inductance of the locomotive motor when this is switched off (remember, the motor is pulse driven). A bonus of free-wheeling diodes D_3-D_6 that act in conjunction with C_4 is the virtual elimination of wheel sparking. This in turn means less interference in the electronic circuits and less contamination of wheels and rails.
The lower supply voltage for the logic circuits is derived via D_2, R_8, D_1, and C_5. This voltage must lie between 3V and 6.3 V (which is the maximum permissible input voltage of IC_5). The value chosen in the present circuit is 5.5 V because that is the rating of the possibly required external buffer capacitor. If the supply fails, and C_5 is retained as the only buffer, the circuit stores the last received data for about 5—10 seconds. This period is determined primarily by the current drawn by IC_1 (25-50 μA) and the leakage current through D_1. The use of an external buffer capacitor lengthens the period and this may be essential where locomotives are used in conjunction with the Marklin digital system and a track with conventional block protection.

Two-rail adaptor

Since Marklin uses a three-rail system, it is always clear which of the connections in the locomotive are the brown lines

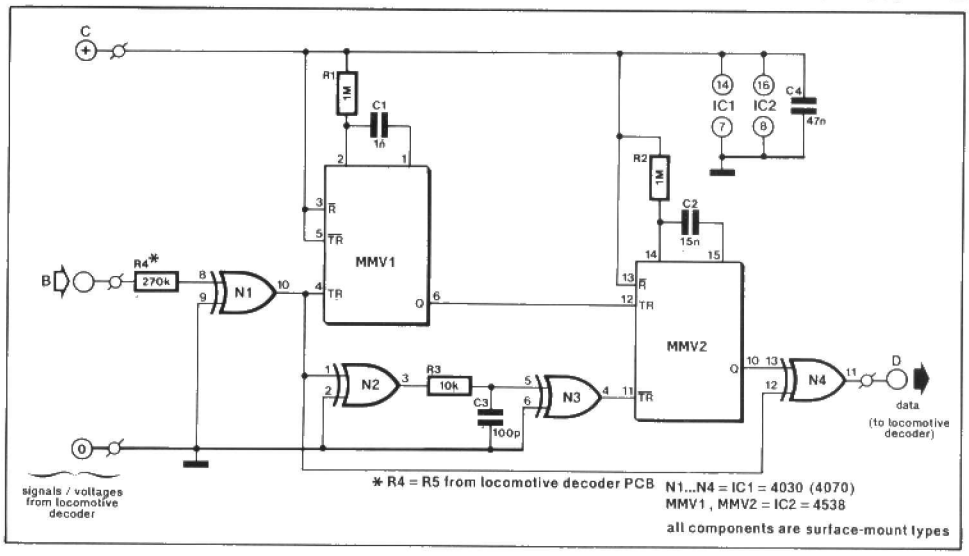
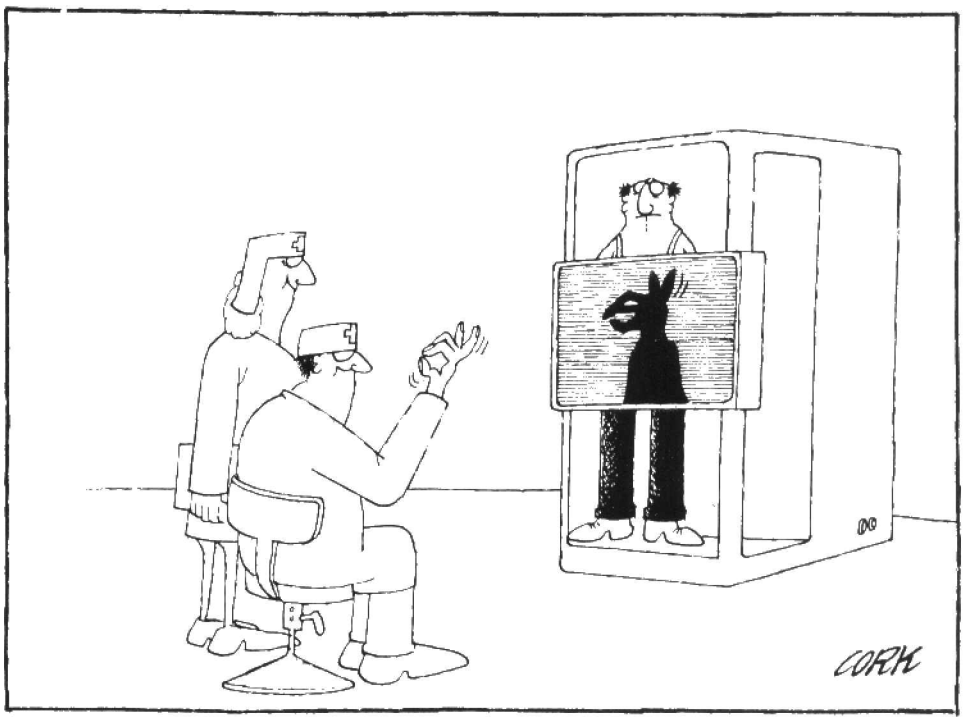


Fig. 17. The circuit diagram of the two-rail adaptor.

(outer rails) of the system and which the red line (centre rail). This is not so in two-rail systems, where the polarity of the supply lines can be reversed by reversing the locomotive. This is immaterial with regard to the main power supply, but it causes complications as far as the data are concerned.
In the Marklin system, data are present on all three lines, but those on the red line are inverted with respect to those on the brown lines. The two-rail adaptor determines which is the red line and which are the brown lines and inverts the data where necessary.
The circuit diagram of the adaptor is shown in Fig. 17. Multivibrator MMV_1 detects the intervals between the data bytes. If its input is logic high during the interval, the connected supply line is brown, the data on which must be inverted. This is done by retriggering MMV_2 at the start of the next data byte which causes N_4 to (continue to) work as an inverter.
If the supply polarity changes, the red line is connected to the input of MMV_1, MMV_2 is no longer retriggered, and N_4 ceases to invert the data.
If the supply polarity changes at precisely the time a byte is transmitted, the data comparator in the locomotive decoder prevents the acceptance of a partially inverted byte.
The supply for the two-rail adaptor is derived from that of the locomotive decoder.
The construction of the locomotive decoder and two-rail adaptor will be described in next month's instalment.

Corrections

In the parts list of Part 1 (p. 44), T_1, a Type BC547 is omitted.
In Fig. 8, bit 9 at the top is logic 1 and not logic 0 as indicated.



PRACTICAL FILTER DESIGN (3)

by H. Baggott

A practical filter may be designed in a number of ways. It may be a passive type, constructed from resistors, capacitors, and inductors, or it may contain active components that take the place of inductors. Both these types are considered in this third part in the series.

The design of a practical filter depends on the requirements, the application and the available components. Simple filters are normally designed as passive types. None the less, complex filters may very well be of the passive type also, although the size of the necessary inductors is often a severely limiting factor. Since the value of inductors for low-frequency filters is often quite high, the modern tendency is to use active filters for low-frequency applications. However, cross-over filters for use in loudspeaker systems are often still of the passive type. In this article a number of filter designs complete with formulas for their practical realization will be described. These considerations will be confined to low-pass sections, since these form the basis of all other types. High-pass filters are a direct derivative of low-pass sections, while band-pass networks with a fairly wide response are constructed from a mix of low-pass and high-pass sections. Band-pass filters with a narrow response and all-pass filters will be considered later in the series.

Passive low-pass sections

Two versions of passive low-pass section will be considered:

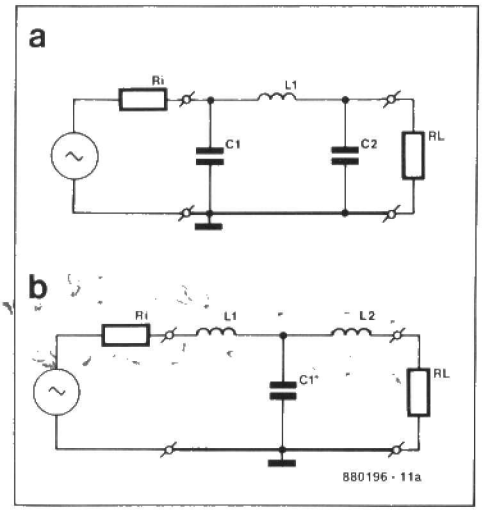


Fig. 12. Passive filters with equal input and output impedances (Ri = RL): (a) π-type; (b) T-Type

- One whose input and output terminating impedances are equal (primarily used in h.f. applications). This type of filter is normally constructed in a π- or T-shape as shown in Fig. 12. A number of sections may be simply cascaded to form a C-L-C-L-C or an L-C-L-C-L network. Note that Ri is the internal source resistance.
- One that is connected to a signal source with negligible internal resistance and terminated into an impedance RL.

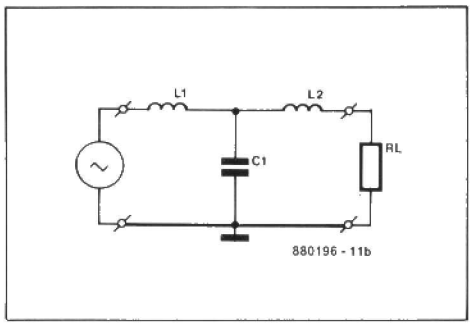


Fig. 13. Passive filter connected to a source of negligible internal resistance and terminated in RL.

This type, normally constructed in a T-shape (see Fig. 13), is used primarily in low-frequency applications. Several sections may be cascaded to form an L-C-L-C-L network.

For clarity's sake, the sections are shown with an odd number of capacitors and inductors, although an even number is perfectly permissible (for instance, one capacitor and one inductor).

Other combinations of input and output impedance are, in principle, possible, but the two versions described here will suffice for the vast majority of passive filter applications.

The tables, given later in the series, show the component values for each of the two versions at a frequency of 1 Hz. The value of the inductor, L', at the required cut-off frequency is calculated from:

$$L' = LR_L/f \qquad [7]$$

and that of the capacitor, C', from:

$$C' = C/fR_L \qquad [8]$$

Active low-pass sections

Configuration with voltage follower. The simplest form of active low-pass section, shown in Fig. 14, uses an opamp connected as voltage follower. Amplification in the pass-band is unity. This type of filter should be driven from a signal source with very low internal impedance. The output impedance of the filter is also very low. Fig. 14a shows a two-pole version (one pair of conjugate poles), whereas Fig. 14b illustrates a three-pole type (one pair of conjugate poles and one real pole). The three-pole version can be used only in odd-order layouts in view of its single real pole.

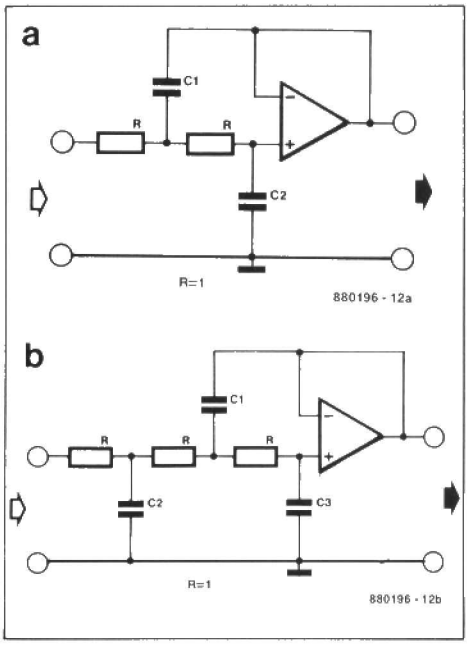


Fig. 14. Active filter with opamp connected as voltage follower: (a) two-pole type and (b) three-pole version.

Depending on the required function, a number of these sections may be cascaded. For instance, for a sixth-order filter three two-pole sections need to be connected in series; for a fifth-order network, a two-pole section is connected in series with a three-pole version. A function requiring an odd number of poles may also be realized with a number of two-pole types followed by a passive *RC*

network as shown in Fig. 15a. If the input impedance of the circuit connected to the filter output is so high that it may be ignored, a buffer terminating the *RC* network is not needed. In other cases the circuit of Fig. 15b may be used, in which the amplification of the opamp may be set with the aid of resistances R_A and R_B (amplification $A = 1 + R_A/R_B$).

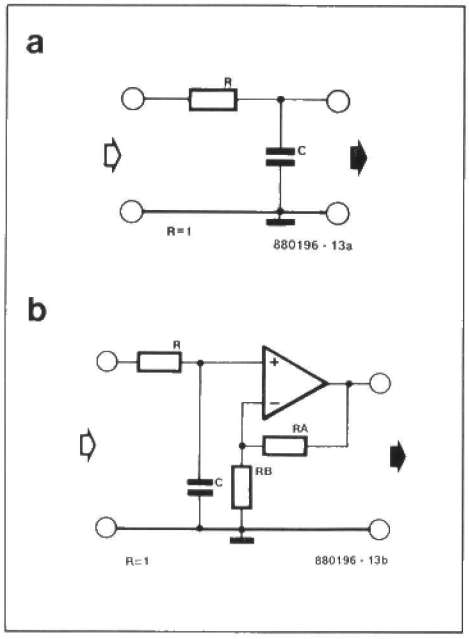


Fig. 15. A real pole may be obtained from a simple *RC* network (a). The addition of an opamp (b) enables buffering and amplification.

The transfer function of the two-pole filter in Fig. 14a is:

$$T(j\omega) = 1/[C_1C_2(j\omega)^2 + 2C_2(j\omega) + 1] \quad [9]$$

in which all resistors have been given a value of 1. The value of the two capacitors as a function of the real and imaginary part of the complex pair of poles may be computed from:

$$C_1 = 1/2\pi\alpha \quad [10]$$

$$C_2 = \alpha/2\pi(\alpha^2 + \beta^2) \quad [11]$$

The transfer function of the three-pole network in Fig. 14b is:

$$T(j\omega) = 1/[C_1C_2C_3(j\omega)^3 + 2C_3(C_1 + C_2)(j\omega^2) + (C_2 + 3C_3)(j\omega) + 1] \quad [12]$$

In this equation, the values of the capacitors can not be given simply as a function of α and β. Their computation really needs to be done with the aid of a computer.
In a network with one real pole, the value of the capacitor is given by:

$$C = 1/2\pi\alpha \quad [13]$$

The values of the capacitors in two- and three-pole filters with a voltage follower are calculated from the tables ($f = 1$ Hz!) at the required cut-off frequencies. This is done by choosing a value for R and determining the required cut-off frequency and then calculating C' from

$$C' = C/fR \quad [14]$$

When two or more sections are cascaded, the value of R need not be the same for each section, but that of the frequency must, of course, remain the same throughout.
If a number of two-pole sections is to be combined with a section with one real pole (Fig. 15a or Fig. 15b) to obtain an odd-order filter, bear in mind that the tables give capacitor values for the last two-pole section and the passive section that are different from those given for the three-pole filter.

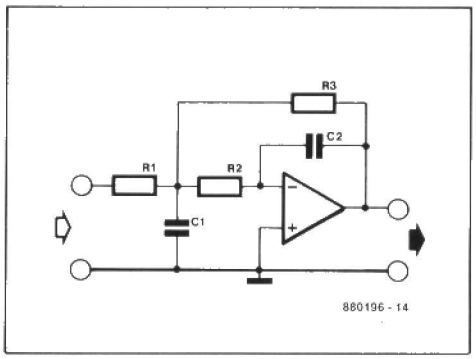


Fig. 16. A two-pole filter with adjustable amplification.

Two-pole filter with amplification. The two-pole section in Fig. 16 offers variable (preset) amplification. The various components are calculated from:

$$C_1 = (A + 1)(1 + \beta^2/\alpha^2) \quad [15]$$

$$C_2 = 1$$

$$R_1 = \alpha/2\pi A(\alpha^2 + \beta^2) \quad [16]$$

$$R_2 = (AR_1)/(A + 1) \quad [17]$$

$$R_3 = AR_1 \quad [18]$$

The computation is usually started by giving an arbitrary (standard) value to C_2 and then calculating the other components from the given formulas.
This type of filter, if desired, may be combined with the other filters described earlier. It is, for instance, possible to create a sixth-order network from two sections as shown in Fig. 14a and one as illustrated in Fig. 16.
State-variable filter. In some applications, the state-variable filter offers definite advantages over the filters described so far. The poles and zeros of this type of filter can be arranged fairly accurately, which in other types is next to impossible owing to the effect the components have on one another. Moreover, the bandwidth and amplification of the opamp have little effect on the filter characteristics. This type of

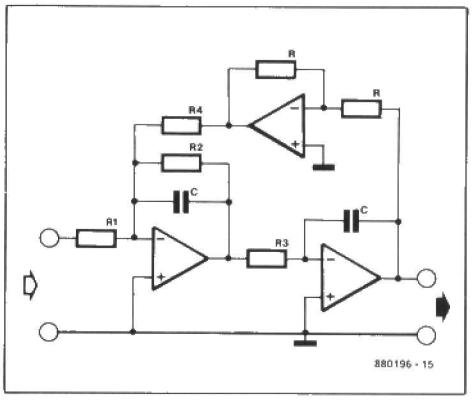


Fig. 17. The state-variable filter is used mainly in applications where the poles and zeros must be arranged fairly accurately.

filter can have some degree of amplification.
The various components are calculated from the following formulas:

$$R_1 = 1/[2\pi AC\sqrt{(\alpha^2 + \beta^2)}] \quad [19]$$

$$R_2 = 1/4\pi\alpha C \quad [20]$$

$$R_3 = 1/2\pi C\sqrt{(\alpha^2 + \beta^2)} \quad [21]$$

$$R_4 = R_3 \quad [22]$$

If the amplification is unity, $R_1 = R_3$.
Here again, the calculation is started by giving C an arbitrary (standard) value, after which the other components can be computed
To finalize the design, the resonance frequency, f_o, and the Q-factor of the filter are calculated for a real cut-off frequency, f, from:

$$f_o = f\sqrt{(\alpha^2 + \beta^2)} \quad [23]$$

$$Q = f_o/2f\alpha \quad [24]$$

The value of R_3 is adjusted to give maximum voltage at the band-pass output of the filter (output of A_1) when a signal of frequency f_o is applied to the input.
Also at the output of A_1, the bandwidth is measured and R_1 adjusted until this corresponds with that taken for the calculation of the Q-factor ($B = f_o/Q$).
It is clear that in the case of a state-variable filter it is advisable to make R_1 and R_3 a series combination of a fixed and a multi-turn preset potentiometer.
Next month's instalment will deal with high-pass sections and their computations.

SEE SEPTEMBER 1989
ACK FOR CORRECTION

APPLICATION NOTES

The contents of this column are based on information obtained from manufacturers in the electronics industry, or their representatives, and do not imply practical experience by *Elektor Electronics* or its consultants.

USING EXTERNAL FEEDBACK TO ACHIEVE FLAT GAIN

by Dan McNamara and William Mueller*

Introduction

One of the classic problems facing the r.f. designer is to build a cascadable amplification stage that has flat power gain over a broad frequency range. The difficulties arise from the gain vs frequency characteristics of semiconductor devices. Up to some frequency fβ transistors exhibit flat gain vs frequency performance. Above fβ the gain of the transistor will drop at rate of 6 dB per octave (i.e. the amplification factor will decrease by ¼ for each doubling in frequency.) Since f is a relatively low frequency (300 MHz typically for Avantek's SAT bipolar process) the designer is usually working in this area of gain rolloff. Thus a "perfectly matched" amplifier (an amplifier with both S_{11} and S_{22} conjugately matched) will also exhibit a 6 dB per octave gain rolloff. If the amplifier is intentionally mismatched to flatten gain, the result will be high VSWRs at either the circuit input or output. The resulting amplifier will not cascade well owing to interactions (impedance mismatch) with driving or load stages.

One solution to this problem is the use of feedback. Feedback allows the designer to trade gain for bandwidth; in essence, through feedback the semiconductor becomes a device with a lower gain and a higher f. The only limitation is that at any given frequency the gain of the feedback amplifier will at best be equal to, and usually several dB less than, the maximum available gain of the original semiconductor. If both parallel (base to collector) and series (emitter) feedback are used simultaneously, the resulting amplifier can have low input and output VSWRs as well as constant amplification over a wide bandwidth.

Avantek's MODAMP™ line of silicon monolithic amplifiers makes use of this technique to achieve good match and flat gain over very wide bandwidths. There will, however, always be times when a circuit is needed that will perform to a still higher frequency before the inevitable rolloff occurs. What can a designer do? One answer is to use more feedback!

Consider the case of the MSA-0885. This device uses minimum feedback to achieve high gains at low frequencies (greater than 30 dB below 500 MHz) while still having useful gain at high frequencies (greater than 10 dB at 4 GHz). Through the application of external feedback to the MSA-0885 it is possible to design a well matched single stage amplifier that will have a flat gain response to beyond 3 GHz.

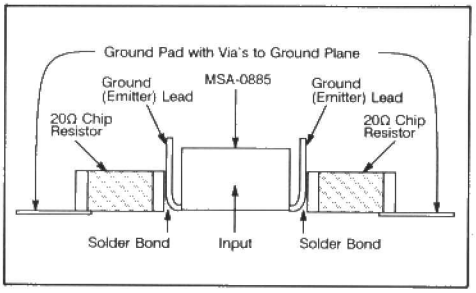


Figure 1. Diagram of shortened ground path.

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VAR
 T1=32          board thickness (mils)
 W1 110         microstrip line width (mils)

CKT
 MSUB   ER=2.55  ET1  T=1  RHO=1  RGH=0    teflon
 MSUB   ER=4.8   ET1  T=1  RHO=1  RGH=0    epoxy glass

MSAC885  AMPLIFIER  (NO FEEDBACK)
 SLC1          1         2                L=.5 C=1000
 MLIN          2         3                W=W1 L=100
 S2PA          3         4       5        A:MSA0885
 VIA           5         0                D1=30 D2=30 HT1 T=1
 MLIN          4         7                W=W1 L=100
 SLC           7         8                L=.5 C=1000
 DEF2P         1         8                A08
MSAC885  AMPLIFIER  (FEEDBACK ADDED)
 SLC           1         2                L=.5 C=1000
 MLIN          2         3                W=W1 L=100
 S2PA          3         4       5        A:MSA0885
 SRL           5         6                R 6.7 L=.5
 VIA           6         0                D1=30 D2=30 HT1 T=1
 SRLC          3         4                R 225 L=1 C=1000
 MLIN          4         7                W=W1 L=100
 SLC           7         8                L=.5 C=1000
 DEF2P         1         8                AMP

FREQ
 STEP          0.1
 SWEEP         0.5       6       0.6

GRID
 GR1           0         40      5
 GR2           -30       0       -5

OUT
 A08           DB[S21]       GR1
 AMP           DB[S21]       GR1
 A08           DB[S11]       GR2
 A08           DB[S22]       GR2
 AMP           DB[S11]       GR2
 AMP           DB[S22]       GR2

OPT
 RANGE         0.1     4
 AMP           DB[S21]>11.5
 AMP           DB[S21]<11.8
 AMP           DB[S11]<-14
 AMP           DB[S22]<-14
```

Table 1. Initial simulation of feedback amplifier.

Initial Simulation

The design begins with a TOUCHSTONE™ computer simulation comparing a standard MSA-0885 amplifier to an MSA-0885 amplifier including additional external feedbck. The file is shown in Table 1.

The simulation starts with a description of the substrate material. In this case information for both teflon-fiberglass (ε = 2.2) and epoxy glass (ε = 4.8) substrates is included (As shown the line for epoxy glass is "commented out" of the program). The microstrip lines are then modelled in terms of their physical dimensions in mils. The MSA-0885 is described by a measured set of S(cattering)-parameters contained in a file named MSA0885.S2P. This file is reproduced in Table 2.

Since these S-parameters are measured in a fixture that connects the MMIC common leads directly for ground, a via is used to simulate the added inductance in the ground path incurred by passing through the pc board. Both blocking capacitor and feedback resistor models include appropriate associated parasitic inductance. Bias networks are omitted as they are assumed to incorporate chokes high enough in value to avoid any impedance matching effects.

Working with this model in the "tune" mode, the designer will quicklu notices several things. First, it should be possible to build an amplifier with 11 dB of flat gain to past 3 GHz with input and output return loss less than 10 dB. Secondly, the bandwidth limitation is set primarily by the inductance associated

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with the emitter feedback. The lower this inductance can be kept, the broader the bandwidth over which the amplifier will function. Thirdly, the improved match of the feedback amplifier will actually improve gain performance beyond the 50Ω power gain of the original MSA-0885 (but not beyond its MAG).

Prototype circuit

A prototype circuit is built, based on the initial simulation. This circuit verifies that the inductance associated with the emitter feedback resistor is the determining element for high frequency gain rolloff. The layout of this initial circuit incorporates an isolated "pad" adjacent to the emitter lead to which both the device lead and the feedback resistor are soldered. Even though the circuit elements are positioned to keep the path length to ground as short as possible, the extra path length introduced by this floating "pad" plus the parasitic inductance of the chip resistor used add 2.2 nH of inductance to the emitter path. This amount of inductance limits the upper frequency at which the amplifier has acceptable performance (less than 1 dB gain rolloff and input and output return losses of more than 10 dB) to below 1.1 GHz.

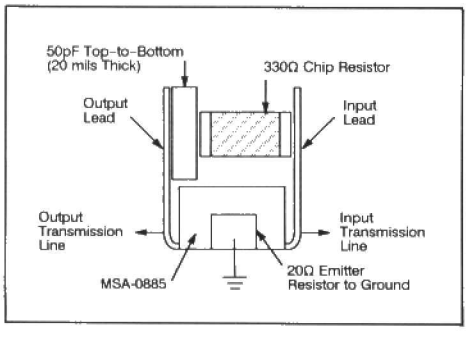


Figure 2. Diagram of feedback path.

An aspect of the circuit that has been omitted from the simulation but warrants closer inspection is the bias choke network. The initial design uses a printed high impedance line in series with the bias stabilization resistor as the "choke" between the bias network and the r.f. circuitry. Measurements show that the impedance of this network is not sufficient to keep the bias network

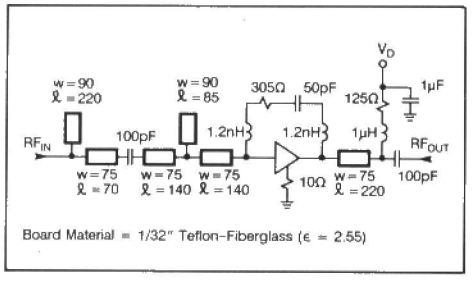


Figure 3. MSA-0885 feedback amplifier schematic.

Id = 36 mA

FREQ.	S11		S21		S12		S22	
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
0.1	0.64	-21	42.29	160	0.015	40	0.61	24
0.2	0.58	39	36.89	144	0.023	50	0.54	-45
0.4	0.44	-65	27.20	120	0.034	54	0.42	-77
0.6	0.36	-82	20.57	106	0.044	53	0.33	-98
0.8	0.31	-95	16.31	96	0.055	53	0.28	-115
1.0	0.27	-105	13.36	87	0.061	51	0.25	-129
1.5	0.24	-125	9.24	71	0.085	50	0.18	-153
2.0	0.26	-147	6.82	56	0.103	47	0.12	-173
2.5	0.29	-159	5.57	48	0.120	44	0.12	180
3.0	0.34	-175	4.51	37	0.130	42	0.09	165
3.5	0.38	172	3.80	25	0.144	37	0.06	172
4.0	0.42	161	3.21	14	0.153	33	0.04	-139
5.0	0.48	135	2.43	-7	0.167	24	0.09	-90
6.0	0.60	102	1.88	-29	0.179	17	0.08	-140

Table 2 .S(cattering)-parameters of MSA-0885.

```
VAR
 T1=32          board thickness (mils)
 W1=75          microstrip line width (mils)

CKT
 MSUB   ER=2.55 HT1 RHO=1 RGH=0   teflon

 MLOC     1                      W=90 L=220
 MLIN     1      2               WW1 L=70
 SLC      2      3               L=.7 C=100
 MLIN     3      4               WW1 L=140
 MLOC     4                      W=90 L=85
 MLIN     4      5               WW1 L=140
 S2PA     5      6      7        A:MSA0885.S2P
 SRL      7      6               R=10 L=.5
 SRL      5      8               R=305 L=1.2
 SLC      8      6               L=1.2 C=50
 MLIN     6      9               WW1 L=220
 IND      9      10              L=100
 RES      10     11              R=125
 SLC      11     12              L=1 C=1E5
 SLC      9      13              L=.7 C=100
 DEF2P    1      13              AMP

FREQ
 STEP     0.1
 SWEEP    0.5    6       0.5

OUT
 AMP          DB[S21]     GR1
 AMP          DB[S11]     GR1A
 AMP          DB[S22]     GR1A
 AMP          K

GRID
 GR1          0      15      1
 GR1A         30     -30
```

Table 3a. Revised circuit file.

FREQ. GHZ	DB[S21] AMP	DB[S11] AMP	DB[S22] AMP	K AMP
0.30000	11.785	-16.032	-16.771	1.086
0.90000	11.790	-13.551	-14.339	1.049
1.50000	11.851	-11.396	-12.980	1.011
2.10000	12.165	-11.083	-13.709	0.999
2.70000	12.265	-14.782	-15.552	0.997
3.30000	12.468	-21.457	-12.540	0.967
3.90000	11.373	-7.962	-11.529	0.875
4.50000	9.165	-4.580	-16.294	0.750
5.10000	6.724	-3.794	-13.627	0.657
5.70000	5.232	-4.729	-6.043	0.614
6.30000	4.075	-8.024	-0.450	0.661

Table 3b. Output of revised circuit file.

from affecting the load impedance presented to the MSA-0885. The easiest way to correct this problem is to replace the microstrip line with a "lumped" element. A 0.1 μH molded inductor has been tried; the parasitics associated with it caused a large resonance at 3.3 GHz. Next a 100 μH chip inductor is used. While it provides extremely flat gain (0.4 dB ripple) out to 3 GHz, the response fluctuates severely beyond 3 GHz. There are high frequency resonances in the bias network that will have to be minimized through the selection of specific values of choke inductance.

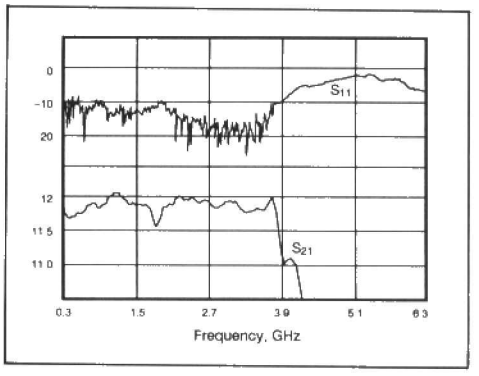


Figure 4a. S_{11} and S_{21} of MSA-0885 feedback amplifier.

Second simulation and final circuit

The TOUCHSTONE simulation is reworked (Table 3) to help analyze the problems observed with the prototype amplifier. Special attention is paid to minimizing the emitter inductance and selecting a choke network that does not create high frequency resonances. Several circuit changes are implemented based on the new simulation.

In order to reduce the parasitic emitter inductance, the physical distance to ground has to be decreased. This is done with a new pc board layout which places the emitter resistor directly against the MSA-0885 ground lead on one end and on top of a via to ground on the other (see Fig. 1). This construction technique results in a glat gain of 11.5 dB out to 3.3 GHz.

Finding the best value for the choke inductance is a complex issue. After trying several inductors of varying values, a 1 μH molded inductor is chosen as it minimizes the high frequency ripple (less

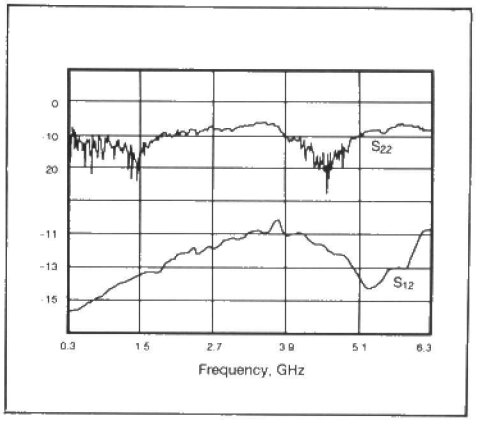


Figure 4b. S_{22} and S_{12} of MSA-0885 feedback amplifier.

than 1 dB) while maintaining the gain at 11 dB. The choice is based solely on observed performance because it is difficult to precisely model the exact parasitics of the choke network.

The inductance associated with the parallel feedback path contributes to the high frequency ripple of the circuit; consequently, the physical length of this path is reduced to a minimum (see Fig. 2 for construction technique). The value of the feedback resistor is also increased to 330 Ω, which provides the best gain while still maintaining an input match with more than 10 dB return loss. Open circuit stubs added to the input transmission line are incorporated in the final amplifier to further improve high frequency input match.

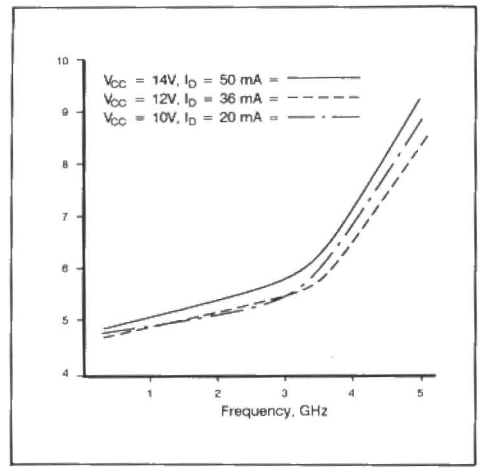


Figure 5. Noise figure vs frequency for MSA-0885 feedback amplifier.

Amplifier performance

A schematic for the final circuit is shown in Fig. 3. Amplifier performance is characterized in terms of S-parameters over the 300 MHz to 6.3 GHz frequency range, with the MSA-0885 operating at a device current I_D of 36 mA. Refer to Fig. 4a and 4b. These measurements show nearly 12 dB of flat (less than 0.5 dB ripple) gain out to 3.8 GHz, beyond which frequency gain rolls off very rapidly. Input and output return losses are on the order of 10 dB over this frequency range. Isolation drops from approximately 15 dB at the low end of the band to 10 dB near 4 GHz.

At the nominal bias of I_D = 36 mA, the circuit has a noise figure between 4.5 and 6.5 dB when operated in the frequency range where the gain remains flat. Reducing the bias to I_D = 20 mA by decreasing the voltage applied to the bias circuit from 12.5 V to 10 V yields no significant changes in noise performance, but results in a lower gain amplifier. When the current is raised to 50 mA (voltage of 14 V), the noise figure increased by roughly 0.25 dB, and the gain performance is comparable to that observed at the 36 mA bias. The noise performance at these bias points is plotted in Fig. 5.

Below 2 GHz, 1 dB compressed power ($P_{1\,dB}$) is significantly influenced by bias. The nominal bias of 36 mA yields the best overall result with a typical $P_{1\,dB}$ of 12 dBm. Above 2 GHz the $P_{1\,dB}$ rolls off fairly quickly (down to 6 dBm at 4 GHz), and is not as strongly influenced by bias level. The measurements of $P_{1\,dB}$ vs frequency as a function of bias current are plotted in Fig. 6.

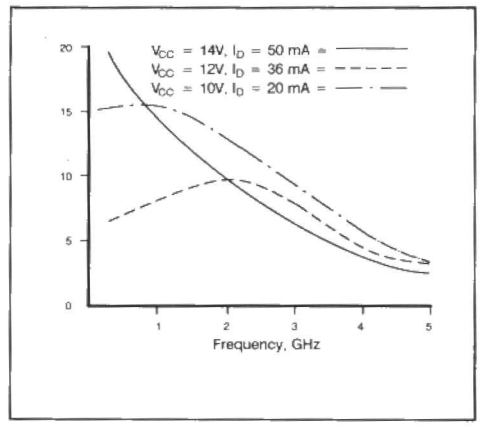


Figure 6. $P_{1\,dB}$ vs frequency for MSA-0885 feedback amplifier.

Conclusion

The design and construction of a broadband flat gain amplifier using MSA-0885 has been discussed. Emitter parasitics and feedback resistor values are the most important considerations in this design to achieve good gain and bandwidth. The final amplifier exhibits nearly 12 dB of flat gain to beyond 3.5 GHz.

Low-frequency performance of this amplifier is determined by the values of blocking capacitor used in the feedback network, as well as the series d.c. blocks in the input and output transmission lines. For all experimental data the low frequency is taken to be 300 MHz. Simulations predict the operational range will extend down to 30 MHz with sifficiently large values of capacitors.

"BATTERY LOW" INDICATOR

by J. Ruffell

Today there are innumerable pieces of equipment that are powered by batteries, both dry and rechargeable. In many cases, it is difficult to determine whether those batteries are still fresh or fully charged or if they need replacing or recharging. Here is a small circuit that monitors the battery voltage and gives an audible warning when that voltage becomes too low.

The indicator described here is small enough to enable it being fitted inside the battery-operated equipment, such as a portable shaver or receiver. It draws a current of not more than 1 mA, so that it does not noticeably increase the load on the battery.

Circuit description

The circuit is based on two opamps that are housed in Type TLC272 chip. Opamp A1, connected as a comparator, compares the battery voltage, applied to the inverting input via potential divider R1-(R3+P1), with a reference voltage of about 4.7 V that is applied to the non-inverting input. Owing to the low zener current, the reference voltage is not always exactly 4.7 V. However, when the battery voltage drops, the potential at the inverting input decreases much more rapidly than that at the non-inverting one, so that the comparator always toggles at the same battery voltage. That voltage may be set very accurately by P1. When the battery voltage is at a normal level, the potential at the inverting input of A1 exceeds the zener voltage. The output of the comparator is then virtually nought. When the zener voltage exceeds the voltage across R3+P1, the comparator toggles, which causes the level at its output to rise to that of the battery voltage. Capacitor C2 is then charged slowly via R5. The potential across the capacitor (at the inverting input of comparator A2) is compared by opamp A2 with the voltage at its non-inverting input. Because of the feedback via R7, that voltage does not have a fixed value, but that does not matter in this circuit. When the potential across C2 has attained a value that is higher than that of the voltage at the non-inverting input of A2, the output of this opamp goes low. Darlington T1, and consequently buzzer Bz1, is then switched on. The buzzer is a d.c. type with built-in oscillator. In this condition, the potential at the non-inverting input of A2 is pulled down a few volts via R7; in other words, there is a degree of hysteresis. Because of that, the buzzer will continue to draw current from C2 until the potential across the capacitor (and thus at the inverting input of A2) has decreased by a few volts. The comparator then toggles so that its output goes high, which renders the buzzer inactive. From then on C2 charges again and the process repeats itself until the quipment is switched off and the battery is replaced or recharged.

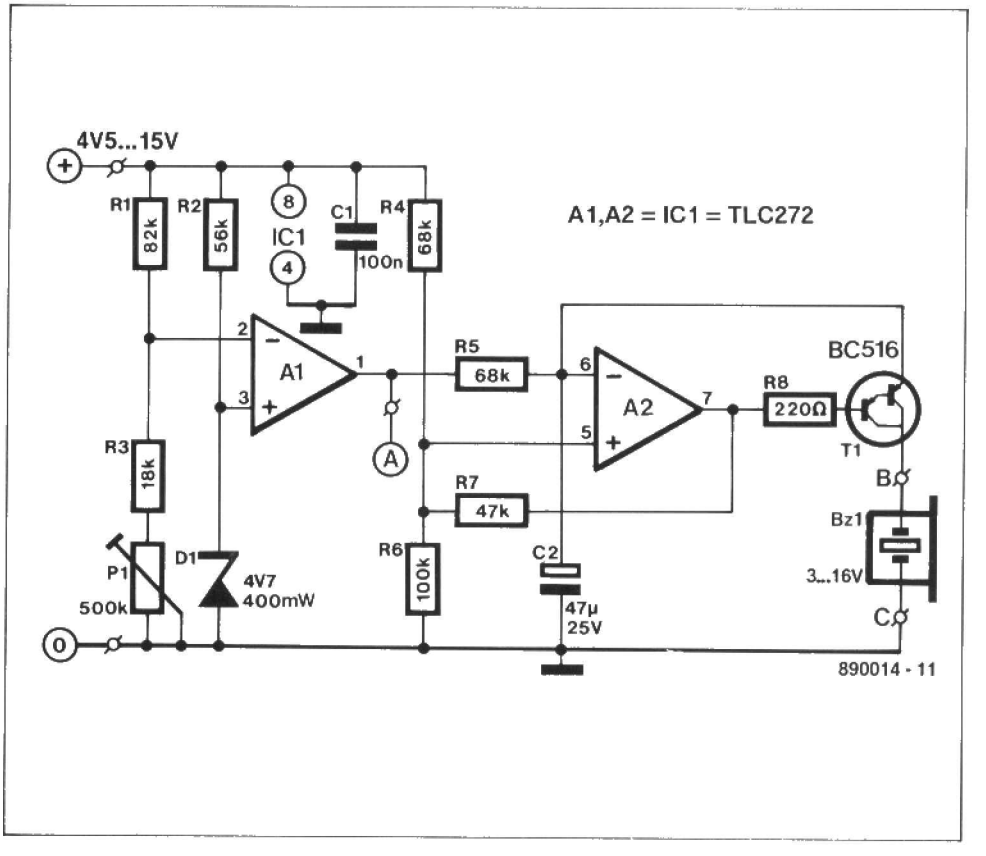
The indicator is suitable for use with battery voltages between 4.5 V and 15 V. When a Type TLC272 IC is used, the circuit draws just under 1 mA. Use of a Type TLC27L2 reduces this to 250 μA at 9 V.

Construction

Since the whole circuit consists of only 15 components, it is easily constructed on a small piece of prototype or vero board. The shape of this should be adapted to the space available in whatever equipment the indicator is to be used.

The circuit is preset as follows. Assuming that the battery voltage is 9 V, the buzzer should start operating at about 7 V. Connect a regulated, variable power supply to the circuit and set its output to precisely 7 V. Turn P1 to maximum resistance. With a multimeter, measure the voltage at the output of A1 (test point A): this should be virtually nought. Slowly turn P1 until the output voltage of A1 suddenly rises to 7 V: this is the correct setting of P1. Within a few seconds, the buzzer should sound.

The indicator can then be fitted into the relevant equipment. Its battery connections should be soldered to suitable take-off points behind the on-off switch.



EPROM-CONTROLLED TIME SWITCH

by J. Vinckier

Time switches can take many shapes. Where apparatus has to be switched on and off at regular intervals, a simple electronic switch will suffice. This article describes such a device that is controlled by a suitably programmed EPROM. It has battery back-up to ensure continued operation in the case of mains failure.

The circuit consists essentially of three parts: a crystal-controlled time base, IC1 and IC2; an address counter, IC4; and an EPROM, IC3.

The time basis is controlled by a 32.768 MHz crystal, X1, which is of a type frequently used in quartz watches and clocks. The 14-stage counter on board IC1 divides the oscillator signal to 2 Hz. That signal is fed to a second counter, IC2, whose Q6 output is connected to address counter IC4. The frequency of the signal at Q6 is 1/64 Hz: the address counter therefore receives a pulse every 64 seconds, upon which it increases its content by 1.

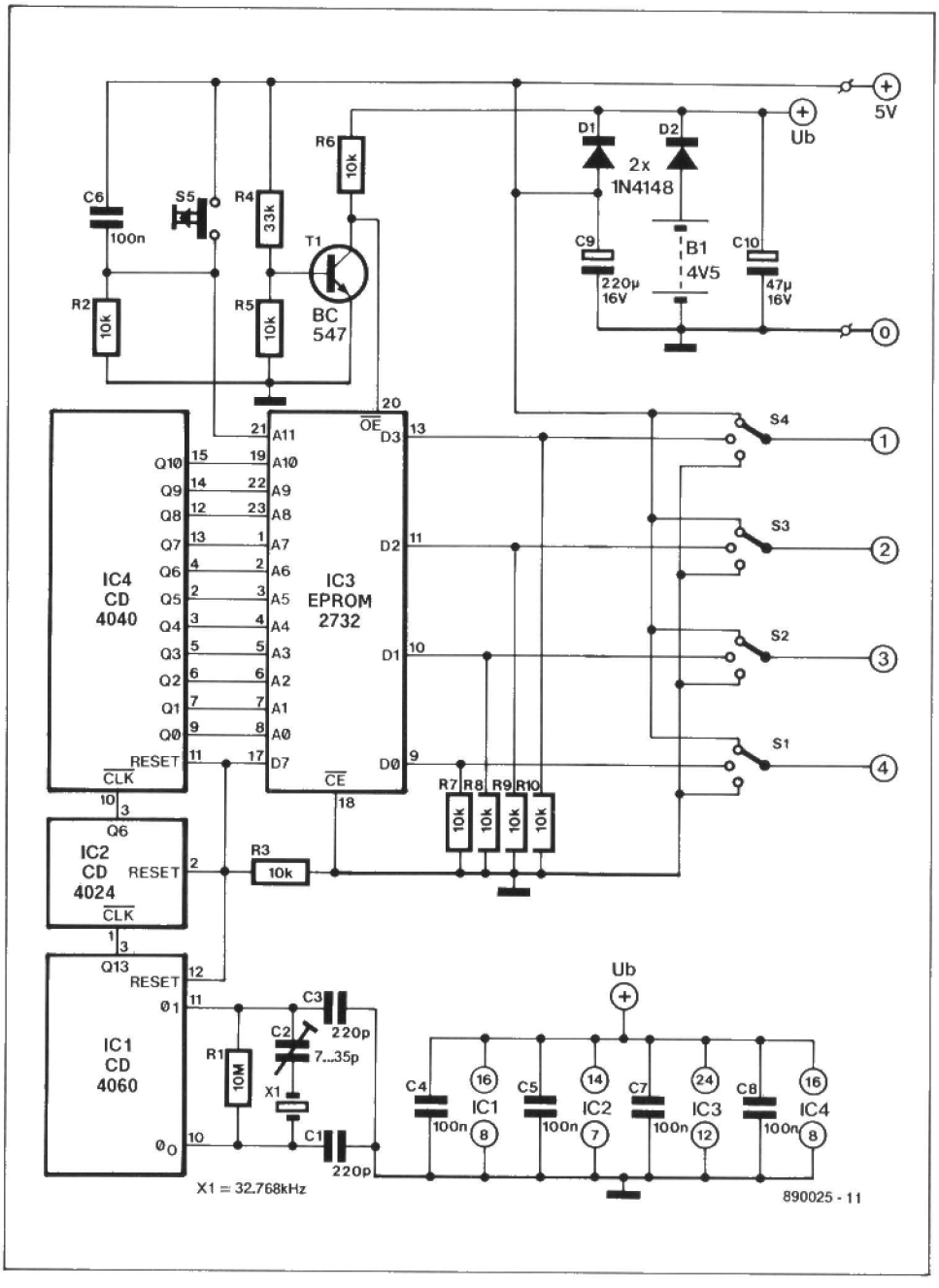
The Q0—Q10 outputs of the address counter are connected to address lines A0—A10 of the Type 2732 EPROM. After 1,350 clock pulses, that is, 24 hours, the address counter must be reset to 0. For that purpose, data output D7 of IC3 is connected to the reset inputs of IC1, IC2 and IC3. At address 1350 in the EPROM, a logic 1 is programmed at bit position 7, so that when this counter position is reached, all counters are reset to 0.

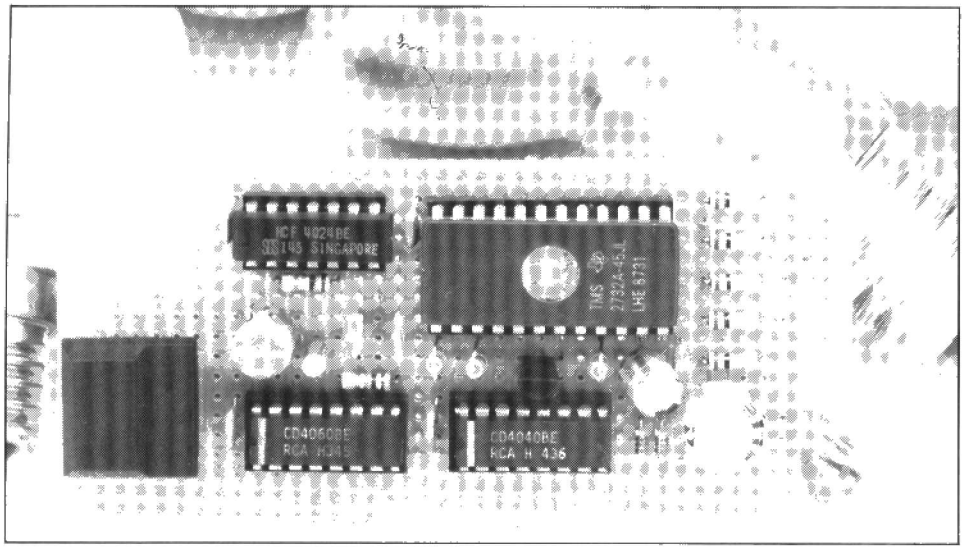
Data lines D0—D3 of the EPROM are used as control outputs, so that up to four different apparatuses may be controlled, each at the same or different times. Depending on the data at memory positions 0—1349 in IC3, these outputs are logic 0 or logic 1.

To enable manual control of the apparatuses, each output is provided with a three-position switch, S1—S4. The switches make it possible for an apparatus to be switched on, switched off, or to be connected to the time switch. The on and off switching may also be done with the aid of relays or electronic switches (optocoupler with triac). In the latter case, take great care to ensure good electrical isolation and a safe construction.

The supply for the switch may be obtained from a mains power supply with possibly a 5-V regulator. In case of mains failure, there is a 4.5-V back-up battery, B1. In that condition, only the four ICs remain powered to ensure the continued running of the clock. However, T1 disconnects the outputs of the EPROM to limit the total current drawn to a minimum. During normal mains operation, T1 is switched on via the +5 V line, which causes the $\overline{OE}$ input of IC3 to go low, so that the data are present at the EPROM outputs. During mains failure, T1 is switched off and the $\overline{OE}$ input is high.

Spring-loaded switch S5 is provided to reset the time switch manually at any





Time	RT	Address	D7	D6	D5	D4	D3	D2	D1	DØ	Data (hex)
0800	0000	0	0	0	0	0	1	0	1	0	0A
0900	0100	56	0	0	0	0	1	0	1	1	0B
1000	0200	113	0	0	0	0	1	0	0	1	09
1830	1030	591	0	0	0	0	0	1	0	1	05
1930	1130	647	0	0	0	0	1	1	0	1	0D
2000	1200	675	0	0	0	0	1	1	1	1	0F
2030	1230	703	0	0	0	0	1	0	1	1	0B
2100	1300	731	0	0	0	0	1	0	1	0	0A
2200	1400	788	0	0	0	0	1	0	0	0	08

0759	2359	1349	0	0	0	0	1	0	0	0	08
0800	0000	1350	1	0	0	0	1	0	0	0	78

		4095	1	0	0	0	1	0	0	0	78

given time: this has to be borne in mind during the programming. It is thus, for instance, possible to arrange the programming to start at 8 o'clock in the morning. Reset switch S5 is then pressed at 8 o'clock next morning and from then on the programming will ensure that all instructions are carried out correctly.

Construction and programming

The circuit may be constructed on a piece of prototyping or vero board. Even the batteries and switches may be mounted on this board. It is, however, strongly advised to fit the mains-carrying parts, including any relays (mechanical or electronic) on a separate board. Note, however, that a prototyping board is not safe for this purpose. The low-voltage and mains-carrying parts may be mounted on the same board if they are electrically well separated by the removal of some tracks and solder pads between the two sections.

Programming

It is possible to calculate the switching times by hand and a simple calculator. For example,

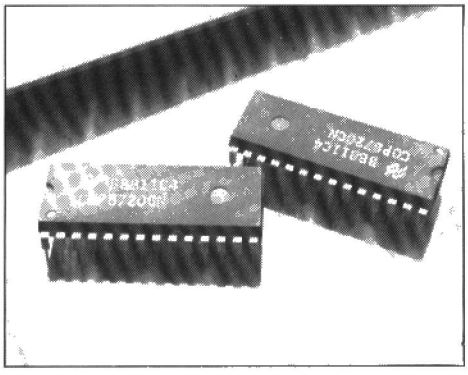
- start time (address Ø) - 0800 h;
- output 1: on 0900 h, off 2100 h;
- output 2: on 2000 h, off 2200 h;
- output 3: on 1830 h, off 2030 h;
- output 4: off 1830 h, on 1930 h.

First tabulate the relative times, that is, the periods between the start time and the switching times. The EPROM address is then computed by converting the relative time (RT in the table) into seconds and divide the result by 64. The examples above are worked out in the table. Note that the memory positions between two addresses must be filled in with the last stated data, for instance, the addresses 1 to 55 must be given the same data as those for address 0. It should be borne in mind that all addresses from 1350 onwards must have a 1 at data bit 7 to ensure that the reset function operates correctly.

NEW PRODUCTS

Controllers with EEPROM

National's new, low-cost COP8720 series of 8-bit microcontrollers, available from Abacus, have 1 kbyte of EEPROM on board, in addition to a RAM cache.

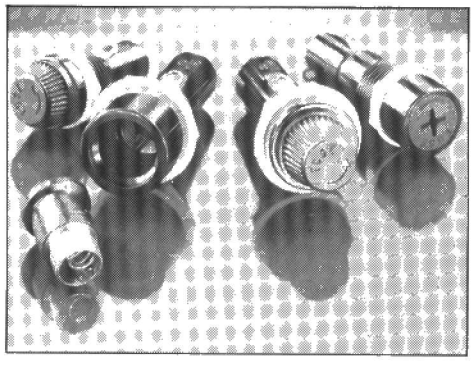


The EEPROM program storage area is complemented by 64 bytes of EEPROM for data storage and 64 bytes of direct-access RAM, which has a resident Stack Pointer. Operating at a clock rate of 20 MHz, the new controllers will execute a complete instruction cycle in 1 μs.

Abacus Electronics Ltd • Abacus House • Bone Lane • NEWBURY RG14 5SF.

Low-cost fuseholders

The new, low-cost range of panel-mounted fuseholders from Rendar has UL and CSA approval.



Compatible fuse sizes are 5.2×20 mm and 6.35×31.8 mm. Current rating is 10 A at 250 V a.c. Contact resistance is 10 mΩ (max) at 1 A d.c. Insulation resistance is 100 MΩ at 500 V d.c.

Rendar Ltd • Durban Road • South Bersted • BOGNOR REGIS PO22 9RL.

Pulse-withstanding resistors

The 'PA Series' of customized pulse-withstanding resistors from Welwyn has applications in the protection of telecommunications equipment from lightning strikes, or the absorption of transient pulses in fluorescent lighting fittings. Each customer's requirements are met in the most cost-effective way by maximizing the pulse-handling capability and at the same time minimizing resistor hot spots. This is achieved by careful selection and matching of raw materials and by the choice of technology and method used to trim the resistor to the required value.

Welwyn Film Resistors • BEDLINGTON NE22 7AA.

DEALING WITH ELECTROMAGNETIC INTERFERENCE

by Alan Baker, BSc(Eng), ACGI, CEng, FIMechE

Electromagnetic interference (EMI), almost ignored about ten years ago, has now become important, primarily because of the proliferation of electronic equipment in aerospace, motor vehicles and other industries.

A feature of such equipment is its sensitivity to electromagnetic emanations in the environment, and it cannot be completely shielded from them. Consequently there is widespread interest in assessing the levels of EMI likely to be encountered in various circumstances and in developing valid methods of testing the susceptibility of different types of electronic systems.

Laboratories devoted to these activities have therefore sprung up worldwide, some for particular industries and others in university engineering departments. The latest, for the automotive industry, is the electromagnetic compatibility (EMC) laboratory officially opened last year for the Motor Industry Research Association (MIRA) at Nuneaton.

This is especially timely in view of the rapid growth of vehicular electronic applications such as ignition systems, engine and transmission management, adaptive and active suspensions, antilock brakes and four-wheel steering. The effect of any malfunction caused by EMI on these items can range from simple annoyance to a catastrophe.

Europe's largest laboratory

MIRA's EMC department is not yet six years old but its early growth rate was so rapid that the need for expansion was already obvious to its then director, Dr Cedric Ashley, before the end of 1984. He subsequently gained financial support from Britain's Department of Trade and Industry, the Department of Transport, the Metropolitan Police in London, and seven companies (Eaton, Ford, Jaguar, Lotus, Lucas, SPA and Saab Scania).

With MIRA's £500 000 contribution there was enough money to do the job properly, resulting in Europe's largest laboratory devoted to this particular sector of automotive technology. The EMC laboratory now has contracts from firms in continental Europe, the United States and the Far East.

Pride of place in the laboratory goes to a large anechoic chamber made of steel and measuring 22 m long × 10 m wide × 7 m high. This is big enough to take the maximum weight of 38 tonnes for articulated trucks, buses or coaches as well as cars. Most vehicles for testing are of course cars but the sizes are useful for them too as accuracy of measurement is impaired if the walls are too close to the source of emissions.

In the interest of repeatability over a broad range of radio frequencies, the chamber walls and ceiling are lined with energy absorbing pyramids which are 1.8 m long and made of polyurethane foam impregnated with carbon.

Regenerative braking system

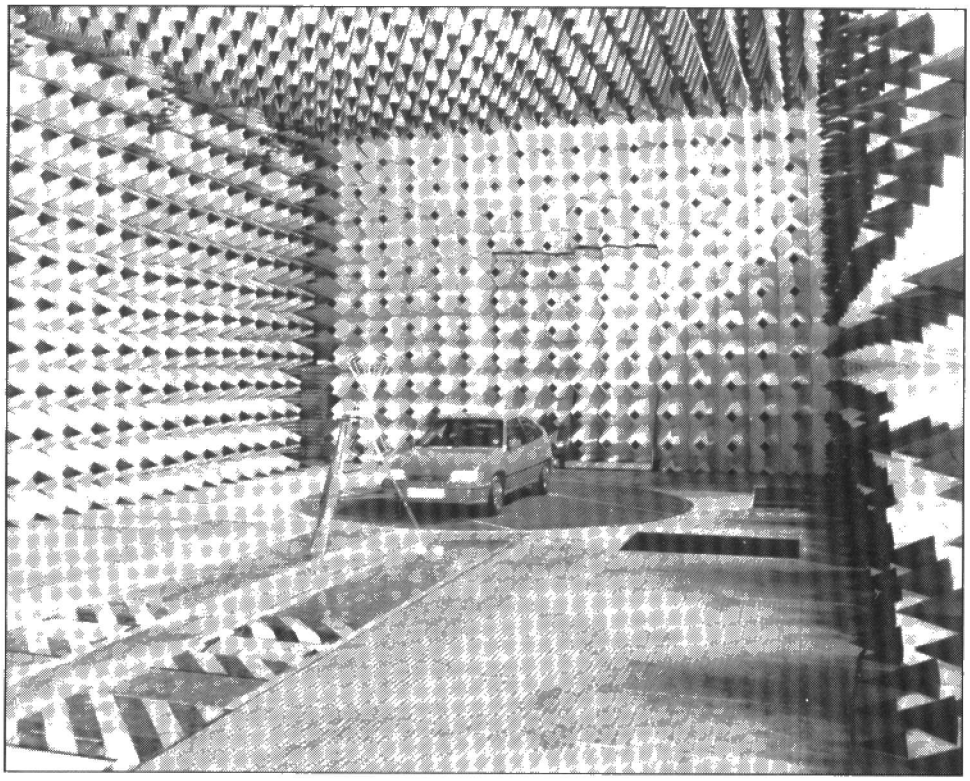
On the floor of the chamber are two sets of vehicle-driven aluminium rolls and a turntable. The rolls drive a large two-axle electric dynamometer installation with a continuous absorption capacity of 150 kW per axle — an input that demands a highly efficient cooling system.

The diameter of the rolls is unusually large at 1.5 m to keep tyre temperature down to acceptable levels, and their maximum peripheral speed is 160 km/h. One of the axles is fixed while the other can be moved to give any desired wheelbase between 2 m and 6.5 m.

The dynamometer operating modes include road load, wheel slip and antilock braking — the latter with decelerations as high as 2 G. A lot of energy has to be dissipated on continuous cycling tests, despite the relatively low mass of the rolls, so the dynamometer incorporates a regenerative braking system.

Braking can be applied to both axles but it is not normally used on the driving one because of possible tyre-rating problems.

The dynamometer, made by Brush Electrical Machinery of Loughborough, enables a wide selection of vehicles to be driven as though on the road while being



The interior of the anechoic chamber which is big enough to take trucks and buses as well as cars. In the foreground are the two sets of 1.5 m diameter dynamometer rolls and beyond them is the turntable with a capacity of 10 tonnes.

subjected to a full spectrum of electromagnetic radiations.
The turntable, also supplied by Brush Electrical Machinery, has a diameter of 6 m and a load capacity of 10 tonnes and is used for static investigations, particularly of vehicle field coupling which can be fully measured. Bulk current absorption spectra obtained on this equipment can be used for — among other purposes — predicting worst case antenna positions for susceptibility tests on the dynamometer, thus saving quite a lot of valuable time.

Other facilities

Alongside the main chamber are the control rooms equipped for both manual and computer controls. MIRA's specialists reckon that this combination of equipment and control systems gives them full competence to evaluate the EMC performance of most common types of vehicle in repeatable and realistic operating conditions over a frequency range from 10 kHz to 1 GHz and with field strengths of up to 200 V/m at 1 m distance.
Outside the laboratory building is a site for measuring whole vehicle radio frequency emissions in actual field conditions to meet statutory requirements. There are also indoor facilities for assessing the susceptibility of electronic sub-systems.
One of these facilities is for bulk current injection, carried out by clamping on electrodes and thereby inducing high frequency currents in the wiring loom, on or off the vehicle, so that their effects on the electrical equipment can be studied. A highly adaptable routine has been developed whereby the testing can take in a single conductor, a group of them or the entire harness.
The susceptibility of electronic equipment to transverse electromagnetic mode (TEM) radiation can be measured on a standard stripline over a frequency range from 10 kHz to 400 MHz at field strengths over 20 V/m. For small objects this apparatus is complemented by a TEM cell with a lower maximum frequency but the capability for considerably higher field strengths of up to 1000 V/m.
Last of the laboratory's facilities is a relatively small non-anechoic screened chamber measuring 5 m long × 3 m wide × 2.3 m high. It is used for giving radiated susceptibility and emission tests to components and sub-systems by the special techniques defined in various European and United States military standards.
Generally, therefore, the MIRA laboratory does not only offer a capability test but provides the world's motor industry with a problem-solving service, ranging from the evaluation of circuit design and the rectification of faults to the complete design of equipment and its final electromagnetic compatibility testing.

EVENTS

IEE Meetings

2 Mar — 18th annual lecture of the Science, Education and Technology Division.
5-10 Mar — Radiowave propagation: third vacation school.
6 Mar — Product liability in Engineering.
6 Mar — Early history of British radio industry.
7 Mar — Artificial intelligence and robotics.
10 Mar — Reliable electronic measurements.
13 Mar — HDTV: how, when, where?
14 Mar — Software bugs: can you ever be free of them?
15 Mar — The application of artificial intelligence techniques to signal processing.
16 Mar — The European engineer.
20 Mar — New advances in optical recording technology.
20-21 Mar — Semiconductor and integrated optoelectronics.
21 Mar — Sir Eric Eastwood Commemorative Lecture: Telecommunications – past, present and future.
22 Mar — Adaptive filters.
29 Mar — The Channel Tunnel and its electrical systems.

Further information on these, and many other, events from: **IEE • Savoy Place • LONDON WC2R 0BL • Telephone 01-240 7735.**

A number of seminars on **Data Communications & Telecommunications, Electronic Engineering and Information Technology** will be conducted this month by **Frost & Sullivan**. Further information from that organization at **4 Grosvenor Gardens • LONDON SW1W 0DH • Telephone 01-730 3438.**

BEAMA is to repeat its successful Contract Conditions seminars at Birmingham and London. The Birmingham seminar will be on 8 March at the Metropole at the National Exhibition Centre and the London one will be on 20 April at the Mount Royal Hotel, Marble Arch.

CADCAM, the Computer Integrated Technology Exhibition will be held from 14 to 16 March at the National Exhibition Centre, Birmingham. Further information from **EMAP International Exhibitions Ltd • 12 Bedford Row • LONDON WC1R 4DU • Telephone 01-404 4844.**

INTERNEPCON and **Semiconductor International** will be held simultaneously at the National Exhibition Centre, Birmingham from 14 to 16 March. Further information from **Cahners Exhibitions Ltd • Chatsworth House • 59 London Road Twickenham TW1 3SZ • Telephone 01-891 5051.**

A one-day seminar entitled **An Introduction to OSI**, followed by a two-day conference, **International Open Systems**, will take place on 20-23 March at the QEII Centre, London. Further information from **Blenheim Online Ltd • Ash Hill Drive • PINNER HA5 2AE • Telephone 01-868 4466.**

A number of courses on **computer engineering, programming, software maintenance and systems development** are run in Britain and Sweden by **ICS Publishing Ltd • Trafalgar House • LONDON W6 8DN • Telephone 01-748 6667** or **ICSP Utbildning AB • Årstaängsvägen 17 • 11743 STOCKHOLM • Telephone (08) 189900.**

A series of one-day seminars *Spotlight Europe 1992* will be held under the auspices of BEAMA at the Selfridge Hotel, Orchard Street, LONDON W1, on March 14 (*Directives of Major Impact*), March 20 (*EEC Funding in Mediterranean Markets*), and March 28 (*Standards and the Mutual Acceptance of Products in the Single Market*). Further information from **BEAMA • 8 Leicester Street • LONDON WC2H 7BN • Telephone 01-437 0678.**

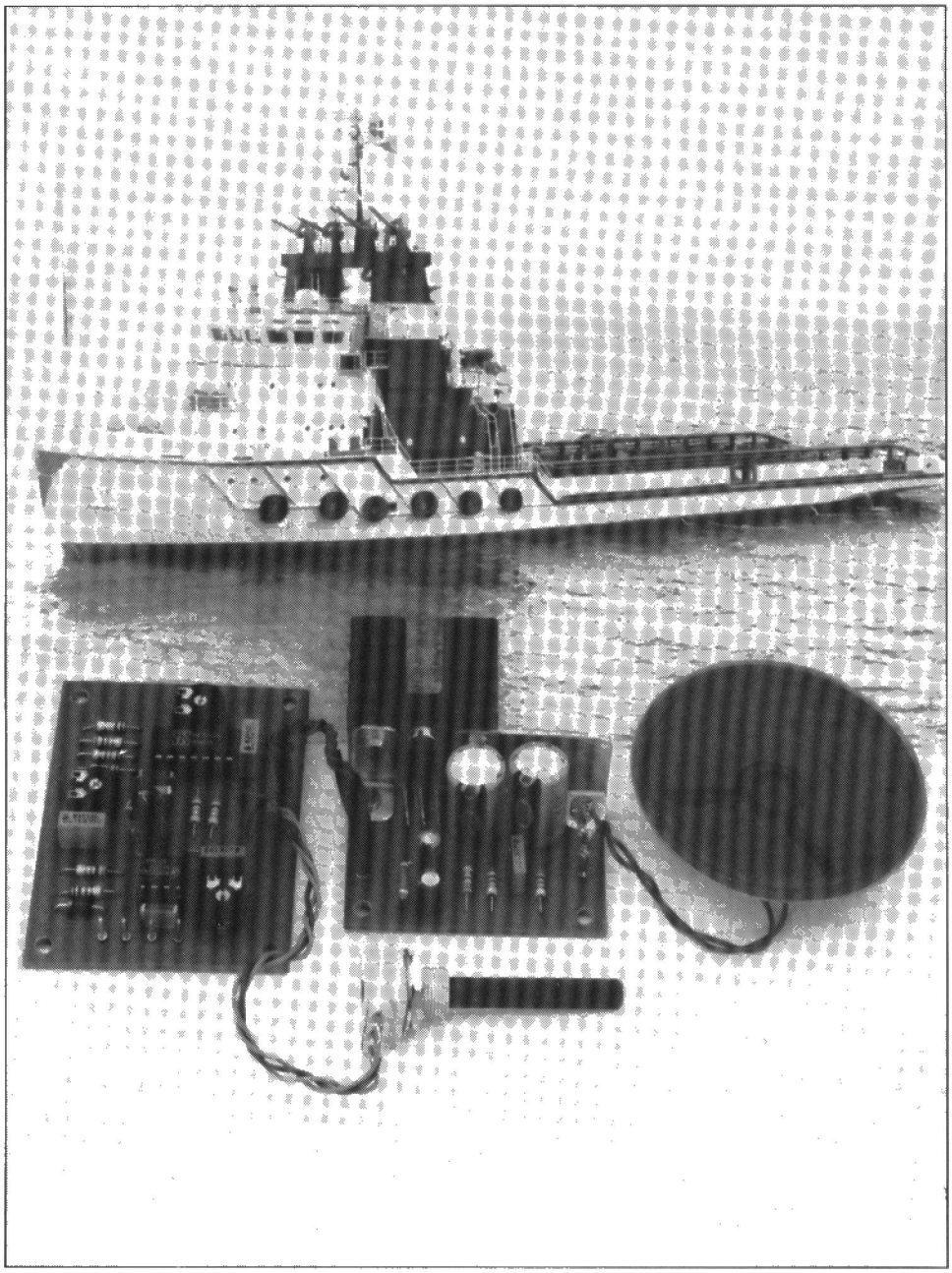
SEMICON Europa 89, the annual meeting of **Semiconductor Equipment and Materials International** will be held at the Züspa Convention Centre in Zürich, Switzerland, from 7 to 9 March. Further information from **Cochrane Communications Ltd • CCL House • 59 Fleet Street • LONDON EC4Y 1JU • Telephone 01-353 8807/1351.**

DIESEL SOUND GENERATOR FOR MODEL BOATS

A low-cost circuit that imitates the sound of a high-power, 10 to 20-cylinder, diesel engine in medium-sized vessels used in, for instance, coastguard and fire brigade services. To obtain a realistic effect in model boats, the design is complete with a powerful AF amplifier, and changes the generated sound both in frequency and character as a function of engine speed.

by T. Giffard

The basic sound of an idling diesel engine as used in medium-size marine craft is a low-frequency hum with a slow beat-like interference that is periodically inaudible owing to the hissing sound produced by the exhaust system. As the engine runs faster, the frequency of the basic sound rises, and is less affected by other sounds.



Sound of an idling engine

The circuit diagram of Fig. 1 shows that the sound generator is built around three square-wave generators. Two of these provide the actual idling sound, the third the effects related to increased speed.
The idling sound is generated by timer IC_1, a Type 556 configured as a double astable multivibrator. The oscillation frequency of both generators is determined by R-C networks connected to pins 12/8 and 6/2 of the chip. The generators' output signals are mixed in emitter-follower T_1, which also ensures a low output impedance. The emitter of T_1 is connected to potentiometer P_3 which serves to set the volume for the AF power amplifier discussed below.
The generator frequencies can be set individually with the aid of presets P_1 and P_2. These are adjusted before wire link A is installed. The presets are first set to the centre position, and then adjusted for minimum frequency difference (zero beat) of the oscillators. One of the presets is then re-adjusted slightly to obtain a slowly varying hum. Some experimentation may be required at this point to obtain a sound of one's liking.

Revving up

The third generator in the diesel sound imitator uses a single timer circuit, the Type 555 in position IC_2. A light-dependent resistor (LDR) has been included in the frequency-determining R-C network of this oscillator. The LDR is illuminated by a small bulb, whose intensity is a measure of engine speed. The faster the engine runs, the more light is detected by the LDR, and the higher the frequency of oscillation. The value of C_4 may be adapted to individual taste. The oscillator frequency at maximum engine speed is adjusted with P_4. An interesting feature of the oscillator is that it actually stops if the motor voltage is nought. This is achieved with R_{10} pulling the input of the oscillator to ground when the LDR is not illuminated, and forms a very high resistance.
Evidently, the lamp connected in parallel with the motor should have the appropriate voltage rating at a relatively low wattage to prevent an undue current drain from the battery on board the model boat. The lamp and LDR are fit-

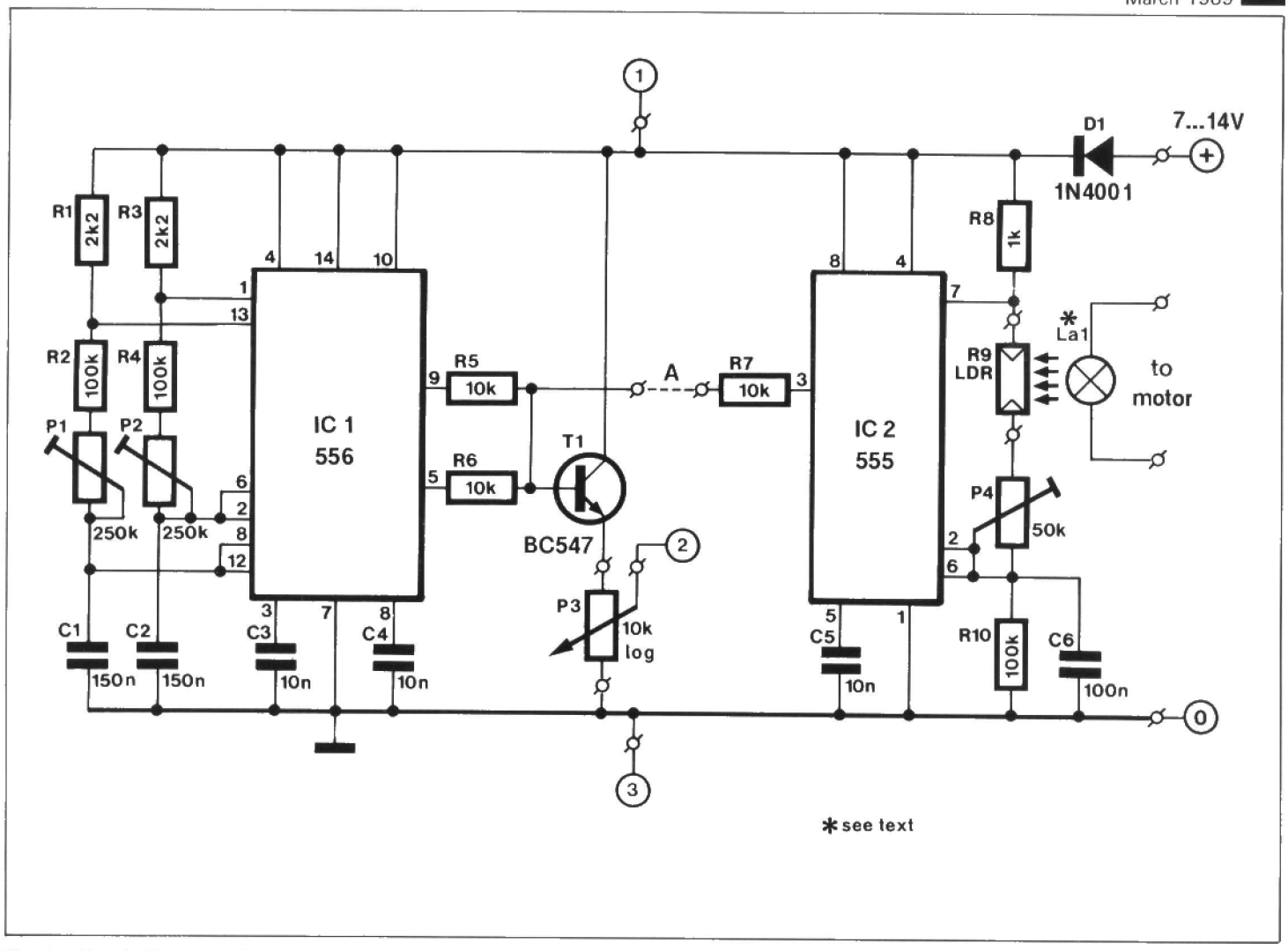


Fig. 1. Circuit diagram of the diesel sound generator.

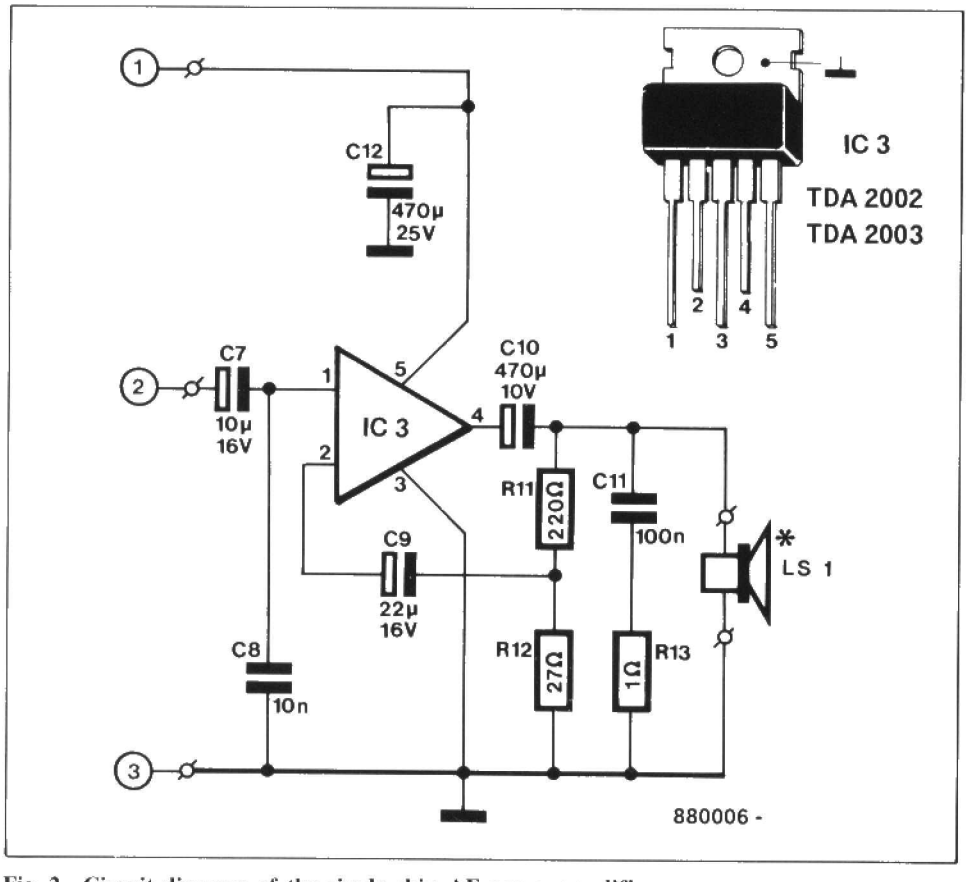


Fig. 2. Circuit diagram of the single-chip AF power amplifier.

ted together in a light-resistant enclosure — a small plastic film container is suitable for most applications. Alternatively, the 'opto-coupler' may be made with the aid of insulating sleeve or tape.

Via R_7, the output signal of IC_2 is fed to the input of mixer T_1. The desired composite sound is obtained by summing of the three oscillator signals.

A separate power amplifier

The circuit diagram of the AF amplifier for the diesel engine imitator is shown in Fig. 2. This unit is built on a separate PCB, and can supply up to 8 W (TDA2002) or 10 W (TDA2003) of output power. The diesel sound generator is purposely split into two, essentially independent, circuits to enable the available space on the model boat to be used in the most efficient manner. Also, the AF amplifier may be used for other applications, such as a siren or fog horn. The load impedance of the AF amplifier should not be less than 2 Ω, so that parallel connection of two 4 Ω loudspeakers is just possible. in most cases, however, a single 4 or 8 Ω loudspeaker provides ample sound output.

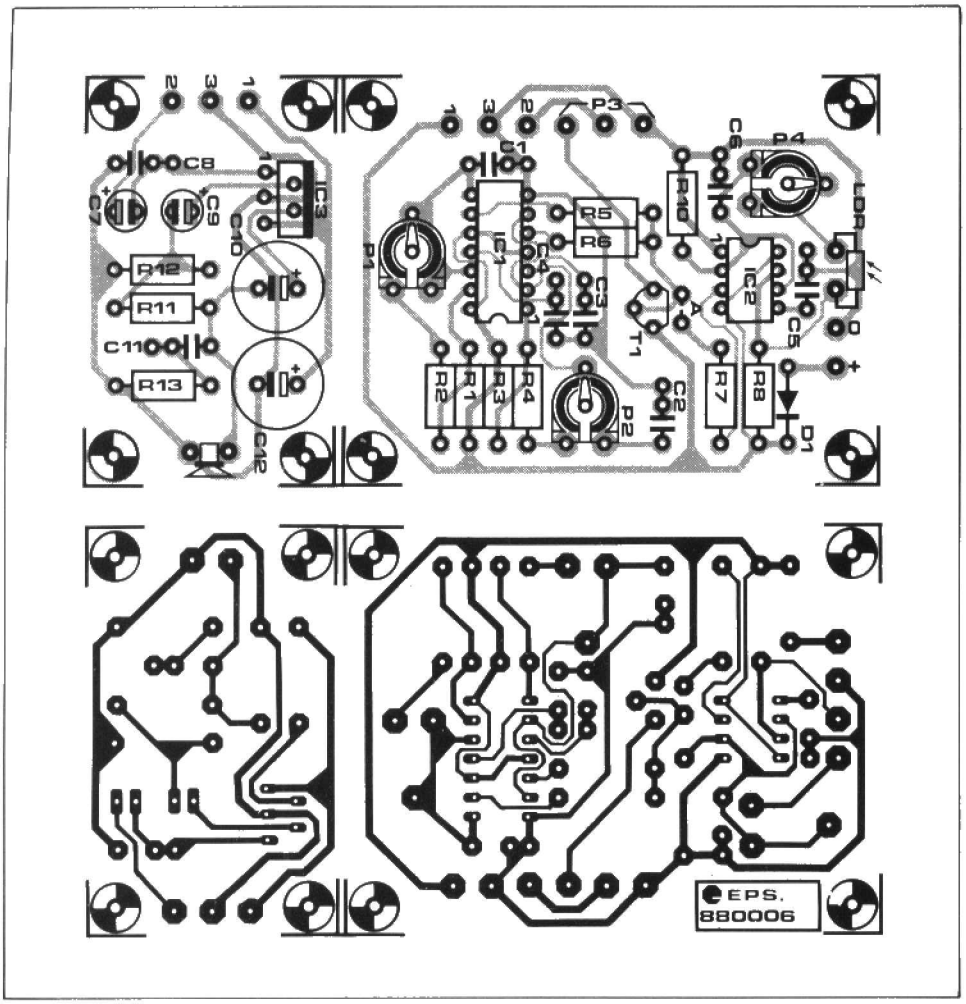


Fig. 3. The printed circuit board for the diesel sound generator is cut in two to separate the sound generator from the AF power amplifier.

Parts list

Resistors (±5%):
R1;R3 = 2K2
R2;R4;R10 = 100K
R5;R6;R7 = 10K
R8 = 1K0
R9 = LDR03 or equivalent
R11 = 220R
R12 = 27R
R13 = 1R0
P1;P2 = 250K preset H
P3 = 10K logarithmic potentiometer
P4 = 50K preset H

Capacitors:
C1;C2 = 150n
C3;C4;C5;C8 = 10n
C6;C11 = 100n
C7 = 10μ; 16 V; axial
C9 = 22μ; 16 V; axial
C10;C12 = 470μ; 25 V; axial

Semiconductors:
D1 = 1N4001
IC1 = 556
IC2 = 555
IC3 = TDA2002 or TDA2003 (see text)
T1 = BC547

Miscellaneous:
Heat-sink for TDA2002 or TDA2003.
Ls1 = 4 Ω loudspeaker; min. 4 W.
La1 = lamp, see text.
PCB Type 880006 (not available ready-made through the Readers Services).

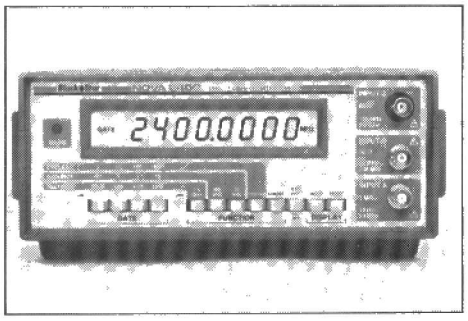
None the less, since the sound produced by the generator is of a relatively low frequency, the loudspeaker should be a fairly large type. Minimum supply voltage for the amplfier is 8 V; it can not be powered from a 6 V battery!

Finally, diode D1 protects the circuit from damage caused by reversal of the supply lines. Current consumption at 12 V is about 300 mA. ◀

NEW PRODUCTS

Budget 2.4 GHz UHF counter

Black Star can now supply the NOVA 2400 UHF Counter Timer, capable of frequency measurement up to 2.4 GHz, period measurement down to 200 ns (0.1 ns resolution), and pulse/event count up to 20 MHz. Where high stability is required, temperature-compensated crystals are available as an optional extra.



The counter is mains or battery operated and has an 8.5 digit LCD that allows a resolution of 10 Hz at 2.4 GHz.

RRP is £299, excl. VAT.

Black Star Ltd • 4 Harding Way • Somersham Road • St. Ives • HUNTINGDON PE17 4WR.

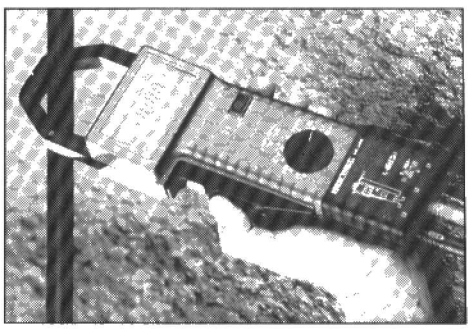
PCB connector

McMurdo have developed a connector for electronic printed-circuit boards that reduces design time and testing problems. The 'Hierarchical Interconnection Technology (HIT)' boards partition what would be complex, high-density circuits into separable, easy-to-mount modules. They also offer significant economies and possibilities to designers of electronic equipment and subsystems.

McMurdo Instrument Ltd • Rodney Road • Fratton Industrial Estate • Portsmouth PO4 8SG.

Six in one

A clip-on ammeter with six separate functions is available from Northern Design. Called Unihall 1000, it uses Hall



Effect techniques in measuring alternating and direct voltage and current, frequency, true power, apparent power, and power factor. Large jaws clamp around the conductor to give no contact, maximum isolation, and negate the need to disturb the insulation or break the circuit.

RRP is £389, excl. VAT.

Northern Design (Electronics) Ltd • 228 Bolton Road • BRADFORD BD3 0QW.

Component Note ACN21 Elektor Electronics "Preamp for Purists"

This component note should be read in conjunction with "Preamp for Purists" published in the October 1988 issue of *Elektor Electronics*. This project is not a complex design and can be adapted to meet many requirements. For simplicity, the relays switching the inputs may be replaced by switches. That will still result in a high-quality preamplifier which will cost very little to build. The performance of the preamp may be improved by the use of even higher grade components than specified in the article.

All components are available from:

AUDIOKITS Precision Components
6 Mill Close • Borrowash • DERBY
DE7 3GU Telephone (0332) 67429

POWER SUPPLIES

Power supplies are the most important part in determining how good your preamp will sound and the heart of the power supply is the mains transformer. Each time you increase the size of the mains transformer you will hear improvements in the quality of sound. The ultimate power supply to use is the Audiokits remote mains transformer as described in ACN 20 (price £1 from Audiokits) but unless low cost is more important to you than sound quality you should use something larger than 8VA suggested in the text! If you decide to use a toroidal transformer you will not save much by using one of the less than 120VA as stocked by AUDIOKITS for the Apex & Virtuoso Preamps.

COMPONENTS

All components connected with the Audio Circuits or with power supplies feeding the Audio circuits affect the sound. The best components are those which change the sound by the lowest amount and these are manufactured to very high quality processes. They are also expensive, sometimes large and the very best parts are only available from limited sources such as Audiokits.

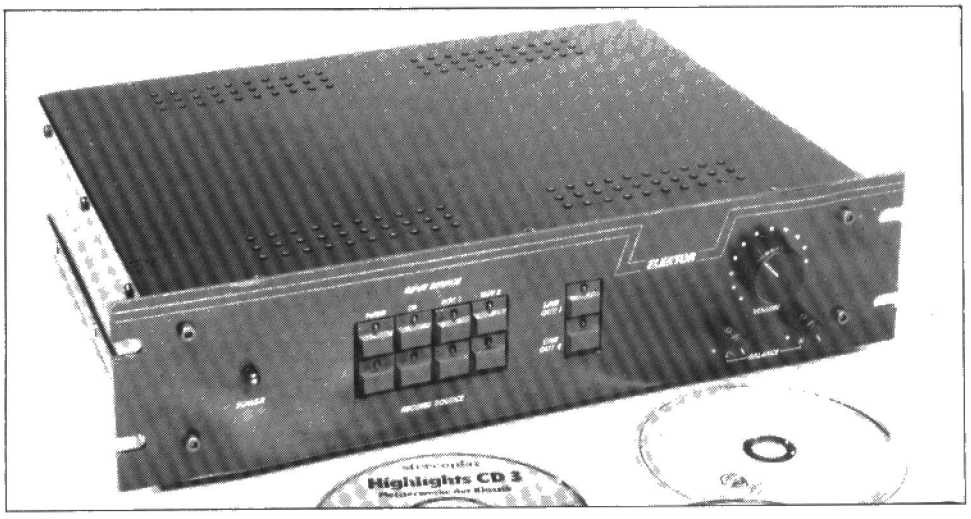
Rectifier diodes can be improved by substituting Fast recovery diodes. Further improvements will result from changing Fast recovery to Schottky diodes.

Resistors can be upgraded by changing to precision types such as Holco precision resistors but best results will be achieved using Vishay Bulk Foil resistors.

Capacitors. There are many grades of capacitors. As a general rule in high quality applications electrolytic capacitors should only be used for power supplies and then should be bypassed by a plastic film capacitor which has less inductance at high frequencies. The four types of plastic film capacitor are polyester (very easy to obtain, small size, los cost) polycarbonate (better quality for slightly higher size & cost) polypropylene (good but more expensive) and polystyrene (very good but large and only easily available in small values).

CABLES

The quality of cables used for signal circuits and power supplies affect the sound quality in a very large way. Cheap cables cause compression of the sound with lack of clarity at extreme high and low frequencies. Some of these faults can be corrected using single core cables (hence their popularity with many designers, manufacturers and users) but for the best results AUDIOKITS stocks a good selection of silver plated copper cables insulated with PTFE.



BUSBOARD

Resistors

R37,37'	10K Holco H8	40p
R38,38'	10K2 Holco H8	40p
R39,41,39',41'	2K21 Holco H8	40p
R40,42,40',62'	48K7 Holco H8	40p
R43,45,43',45'	4K75 Holco H8	40p
R46,46',Ra,Rb	475K Holco H4	40p
	Vishay VSRJ	£5.00
10K	Vishay VSRJ	£5.00
2K2	Vishay VSRJ	£5.00
47K	Vishay VSRJ	£6.00
4K7	Vishay VSRJ	£5.00
475K	Vishay VSR4	£16.00

Capacitors

C33-37,39	100n 7.5mm pitch.	20p

Semiconductors

D1-D6	1N4148	4p

Miscellaneous

ReA-ReD	G2V2 82P 12V	£4.00

Gold Plated Phono Sockets £1.00 (with insulation) £2.00 Heavy Duty £4.00

CONTROL, LINE AMPLIFIER & POWER SUPPLY

R1-9	1M metalfilm 4p
R10,11,16-23	10K metal film 4p
R12,14,24,25	680R metal film 4p
R13,15	4K7 metal film 4p
R26,34	1M Holco H4 40p
R27,28,35,38	22K1 Holco H8 40p
	22K Vishay VSRJ £6.00
R29,37	47K5 Holco H8 40p
	47K Vishay VSRJ £6.00
R30,38	2K49 Holco H8 40p
	2K2 Vishay VSRJ £5.00
R31,39	10K Holco H8 40p
	Vishay VSRJ £5.00
R32,33	47R5 Holco H8 40p
	47R Vishay VSRJ £5.00
P1a,b	10K log Bourns 91A £3.75
P1c	10K log stereo Bourns 91A £11.00

Capacitors

C1-6,11,13,19-24 1μ Polyester 10mm pitch 45p
C7 470μ 40V axial 75p 220μ 40V Mullard 108 £1.45
C89 220μ 40V axial 55p 220μ 40V Mullard 108 £1.45
C10,15, 10m 16V axial 15p 10m 100V Mullard 108 £1.10
C12,14,16,-18,27 100μ 7.5mm pitch 20p
C25,26 47pF Polystyrene 15p LCR FSC 40p
C28-31 22nF 15p

Semiconductors

B1 100V 1A bridge 60p
D1-13 1N4148 4p
D14-D23 3mm L.E.D. in S1-S10
T1,2 BC547C 10p
IC1 4011 MC14011 BCP 45p
IC2 4013 40p Motorola MC 14013 BCP 80p
IC3 4 MC 14028 BCP 75p
IC5 ULN2804A (918010) £2.75
IC6,7 OP227GY £16.00
IC8 7812 70p MC78T12 £3.00
IC9 LM325N £9.00

Miscellaneous

F1 100mA delayed action fuse 20p
K1 Mains input socket £1.00
DIL Heatsink for 1C8 £1.00
S1-S10 Momentary Switch £3.50

Cables

Kimber cable (Red, Blue, Black) £2.50/m.
Audiocable screened cable £4/m
Audiocable 3 core mains cable £12/m

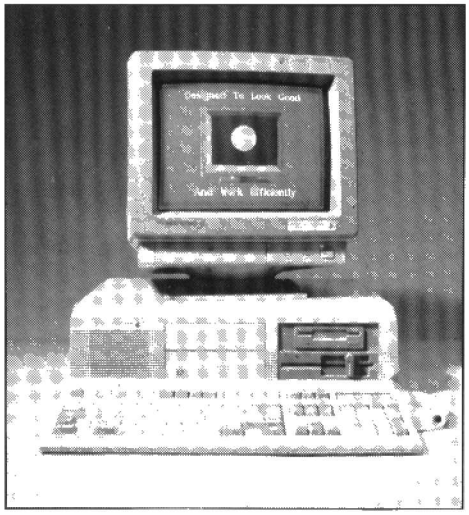
Toroidal Transformer 0-18×2 120 VA £16+£3p&p
0-18×2 300 VA £23+£3p&p

NEW PRODUCTS

New family of PCs

PCML of Esher have a new family of corporate PC and personal workstations. The 80286-based motherboard is designed and built by British Aerospace, while the machine is assembled and marketed in the UK and throughout Europe by PCML.

PCML is aiming the Concorde 286 family at major corporates, including government, defence, and academic institutions. The machines are particularly suitable for high-performance stand-



alone industrial and scientific applications, such as desktop publishing and CAD/CAM, and in the multi-user network file server market. They will, however, also be marketed as fully configured communications servers, combining facsimile, telex and electronic mail, and as personal workstations for applications where data security is a high priority.

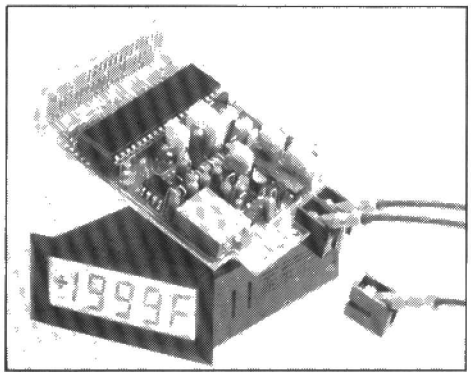
The basic configuration offers a choice of an 8 MHz or 12 MHz processor board and incorporates a 14-inch high-resolution colour monitor and VGA card and a 20 Mb hard disk. The 8 MHz version is priced at £2399, and the 12 MHz machine at £2599.

PCML Ltd • Royal Mills • Esher • Surrey KT10 8AS.

Thermocouple meters

Texmate have introduced a new range of thermocouple meters that are suitable for use with either 'J' or 'K' type thermocouples. They are available in both LCD and LED and can be scaled in either °C or °F.

The TM-35 and TM-35X meters feature thermocouple break detection and indication, Display Hold, Display Test, and Auto Polarity indication. The meters are powered from a 5 V d.c. supply and have a differential input that facilitates operation with both grounded and



ungrounded probes. The unique differential input configuration allows several meters operating with grounded thermocouples to be powered by the same non-isolated 5 V d.c. supply.

The TM-35 is priced at £65.80 and the TM-35X at £67.20 in single unit quantities (excluding VAT and carriage).

Texmate Ltd • Texmate House • P.O. Box 40 • GUERNSEY • Channel Islands.

New layout editor

Labcenter's PC-B *PRO* combines the ease of use of the original PC-B with in-built intelligence and a wide range of editing facilities. The editor is IBM compatible with 512 K RAM, supports EGA, VGA and PC1512 16-colour graphics, and plots on Epson 9-pin dot matrix HPGL compatible plotters.

The PC-B *PRO* is available at £229.95, incl. VAT and p&p.

Integrated auto routeing

Also available from Labcenter is the PC-B *AR*, an auto-routeing system that integrates closely with the PC-B *PRO* for just £170 when bought with that editor or £179.95 when bought later. It is not available, and will not work, on its own. Since auto-routeing is a demanding task for any processor, be it man or machine, Labcenter's philosophy is that the optimum way to work is for the human to do the global planning and for the computer to do the detailed routeing. In operation, the user enters small groups of interconnections with the ratsnest editor, and then invokes OC-B *AR* to do the tedious work of routeing each connection.

Labcenter Electronics • 14 Marriner's Drive • Heaton • BRADFORD BD9 4JT.

Modem on single Eurocard

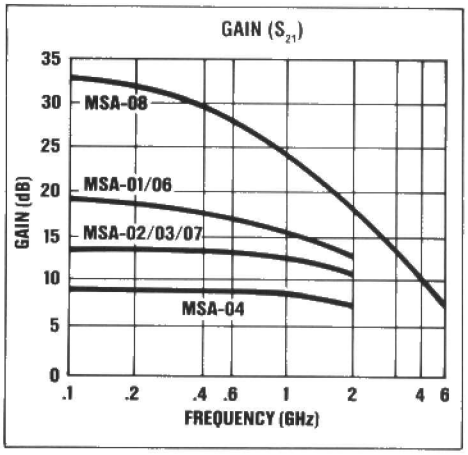
Rockwell's RC2424SME new single-Eurocard modem with on-board computer is available from Abacus.

Based on the versatile RC2424DS modem chip set under control of a R65012 micro, the board will interface with V.22 bis lines at 2400 bps, V.22A and B, V.23, V.21, and Bell 212A and 103 systems. DTE/DCE communications uses the V.25 bis protocol, synchronously or asynchronously. All CCITT modes have automatic identification of protocol and transmission rate.

Abacus Electronics Ltd • Bone Lane • NEWBURY RG14 5SF.

New MMICs from Avantek

Seven new MODAMP™ silicon bipolar microwave monolithic integrated circuit (MMIC) amplifiers in unpackaged chip form have been introduced by Avantek.

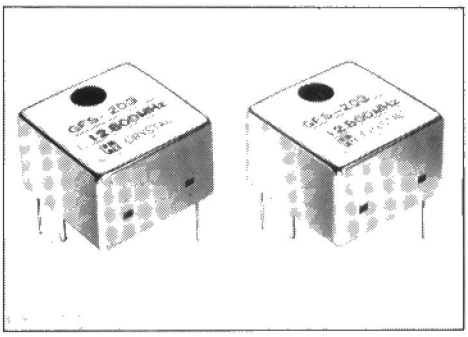


These MMICs are general-purpose, cascadable gain blocks intended for use in narrow- or broad-bandwidth IF and RF amplifier designs. The new family gives the designers of hybrid circuit assemblies a choice of an easy-to-apply, stable and reliable gain block for almost any application from intermediate frequency through microwave.

Wave Devices • Laser House • 132-140 Goswell Road • LONDON EC1V 7LE. For Avantek distributors outside the UK, see the January 1988 issue of *Elektor Electronics*.

Miniature TCXO oscillator

Hz's Type GFS203 Temperature Compensated Crystal Oscillator, one of the smallest in the world (18.5×12 mm) is now available from Total Frequency Control. It is available in the frequency range 5.0 MHz-20.0 MHz. Accuracy is



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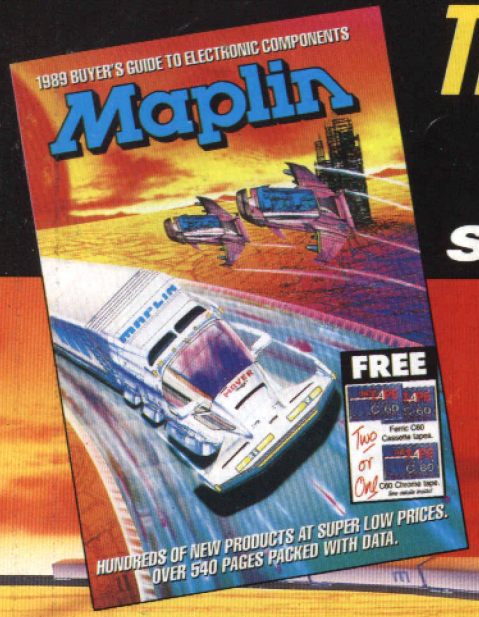

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